DesignCon® 2023

WHERE THE CHIP MEETS THE BOARD

SANTA CLARA CONVENTION CENTER
SANTA CLARA, CA

CONFERENCE:
JANUARY 31 - FEBRUARY 2, 2023

EXPO:
FEBRUARY 1-2, 2023

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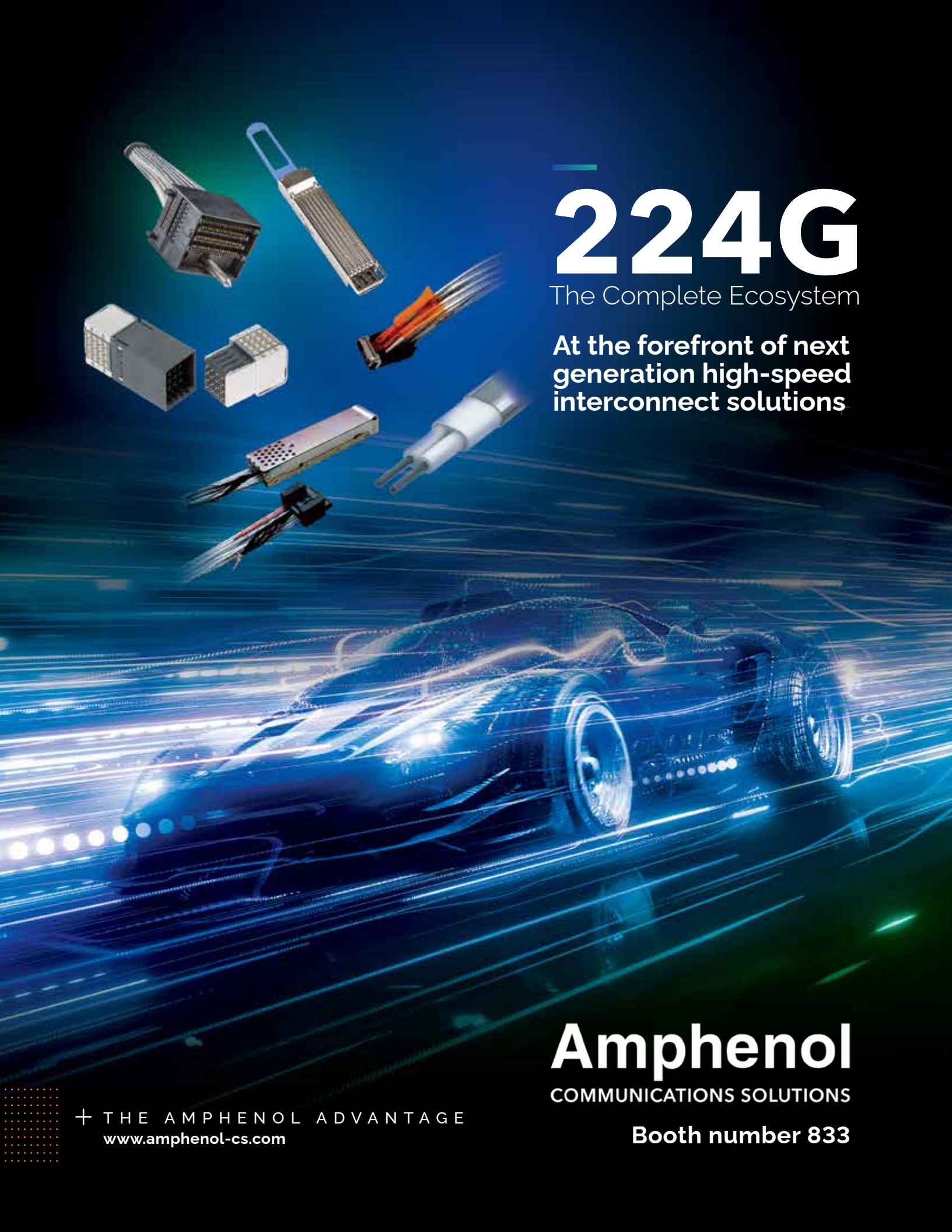
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DESIGNCON® 2023
WHERE THE CHIP MEETS THE BOARD

GENERAL INFORMATION

LOCATION & DATES
DesignCon will take place January 31 - February 2, 2023, at the Santa Clara Convention Center in Santa Clara, CA. DesignCon welcomes Drive World and IEEE Spectrum's Emerging Chips & Markets to this year's event.

CONFERENCE HOURS
Tuesday, January 31, 2023: 9:00 am – 6:00 pm
Wednesday, February 1, 2023: 8:00 am – 5:15 pm
Thursday, February 2, 2023: 8:00 am – 5:15 pm

EXHIBIT HOURS
Wednesday, February 1, 2023: 11:00 am – 6:00 pm
Thursday, February 2, 2023: 11:00 am – 6:00 pm

HEALTH & SAFETY
Health and safety are a top priority at this event. Visit DesignCon.com for up-to-date health and safety information and check the event app for any needed communications during the event.

REGISTRATION
Attendee, Speaker, Media and Exhibitor registration is located in the main lobby. Please present a photo ID when picking up your badge.

Tuesday, January 31, 2023: 8am-7pm
Wednesday, February 1, 2023: 7am-6pm
Thursday, February 2, 2023: 7am-6pm

SMART EVENT
DesignCon is a Smart Event – utilize our event app and event platform for digital enhancements including networking opportunities and exhibitor profiles, featuring white papers, product information, and more. After the in-person event, all attendees, speakers, and exhibitors will still have access to our digital platform where on-demand content from DesignCon will be available at your fingertips through March 3, 2023! There's no need to register again. Your registration for DesignCon carries over to DesignCon's digital enhancements. See page 41 for more information on DesignCon's Smart Event offerings.

WELCOME RECEPTION
Celebrate engineers' contributions to space exploration and enjoy complimentary cocktails, bites, games, and more at DesignCon's annual gathering on Tuesday, January 31, 6:00-8:00 pm in the Santa Clara Ballroom at the Hyatt Regency. Open to all DesignCon pass types. Badges required for entry.
Sponsored by: samtec

CONCESSIONS
Concessions are available in Exhibit Hall A in the Santa Clara Convention Center next to the Chiphead Theater.

CONFERENCE BREAKS
Conference breaks will be provided for paid conference passholders, event committee members, and speakers. The breaks will be located in the conference hallways.

CONFERENCE BREAKFAST
Complimentary breakfast is available on Tuesday, January 31 from 8:00 - 9:00 am in Mission City Ballroom B1 for all paid conference attendees, event committee members, and speakers.

EMERGING ENGINEER BREAKFAST
Designed for engineers with less than 10 years of professional experience, the Emerging Engineer Breakfast runs Thursday, February 2, 8:30 - 10 am in Mission City Ballroom B1. Attendees can connect with peers looking to expand their professional reach, explore companies in electronics offering support for those emerging in their careers, and ask questions of established, highly regarded engineers and authors from the DesignCon community while enjoying a continental breakfast and raffle giveaways.

Sponsored by:
Amphenol UCSC Silicon Valley Extension Professional Education The eecosystem Advanced Electronics Engineering Podcast

The program is subject to change without notice. Informa Markets reserves the right to alter venue, speakers, content, and/or other offerings.

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Samtec's industry-leading signal integrity expertise, full system optimization strategies, and innovative products and technologies provide a path to 224 Gbps performance and beyond.

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BOOTH 939

GENERAL INFORMATION

CONFERENCE NETWORKING LUNCH

Complimentary lunches are available daily from 12:30 - 2:30 pm. for paid conference passholders, event committee members, speakers, and media in Mission City Ballroom B1.

CHIPHEAD THEATER

Check out the specialty programming in the Chiphead Theater featuring panels, training, and more right on the expo floor.

Sponsored by: Amphenol

DRIVE WORLD

DesignCon welcomes Drive World back to the conference, offering an educational track for engineers looking to advance in the growing automotive electronics and intelligence industries. Drive World topics can be found under the session listings in this program. All DesignCon conference passholders have access to Drive World education.

Drive WORLD CONFERENCE

IEEE SPECTRUM EMERGING CHIPS & MARKETS

What will be the technologies driving the next great waves of innovation in semiconductors? Learn about them at this exclusive collaboration between *IEEE Spectrum* and DesignCon, "Emerging Chips & Markets." At this daylong track, you'll hear from the founders, executives, and researchers at the forefront of translating today's breakthroughs into tomorrow's major industries. You'll gain insights available nowhere else and get firsthand briefings about the key challenges in artificial-intelligence accelerators, wide-bandgap semiconductors, micro-LEDs, quantum computing, and more.

Visit page 10 for full details.

IEEE Spectrum

PRODUCT SHOWCASE

See live, interactive demos at exhibitor booths as companies give you a first-hand look at their latest products and features. Demo schedule can be found in the main agenda and on page 48 of this show program.

BOOTH BAR CRAWL

Wind down at daily meet-and-greets around the expo floor, from 5:00 – 6:00 pm, Wednesday and Thursday. Come for the conversation, stay for the bites and beverages. Please note that food will be provided around the expo floor.

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PRESENTATION DOWNLOAD

Use the QR code below to download select speaker presentations. Note: Some presentations are available only for paid conference attendees. Login information will be emailed to paid conference attendees ahead of the event.

DesignCon 2023

WELCOME RECEPTION

Tuesday, January 31, 6–8 pm

Santa Clara Ballroom
Hyatt Regency Santa Clara

Sponsored By:

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Celebrate engineers' contributions to space exploration and enjoy complimentary cocktails, bites, games, and more!

Open to all DesignCon pass types. Badges required for entry.

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WHERE THE CHIP MEETS THE BOARD

GENERAL INFORMATION

APP
This event utilizes a smartphone app to convey any event changes, as well as provide information, such as session details, expo maps, and hours.

Search “DesignCon 2023” in the app store to download, then sign in with the email you used to register along with your confirmation ID.

EVALUATIONS
We value attendee feedback when planning the conference. Conference attendees can evaluate sessions using the below QR code.

INFORMATION DESK
There is an information desk available outside of the main entrance to the exhibit hall and another on the expo floor in the Design News Lounge.

Stop by if you have any questions on the event or need to speak to a member of event management.

INTERNET ACCESS
Wireless internet access is available throughout the building. Please use username “DesignCon” and password “amphenol” for access.

LOST & FOUND
Lost and found is located at Registration.

PUBLIC TRANSPORTATION & PARKING
Information on public transportation and the event’s parking can be found on DesignCon.com’s Plan Travel tab.

MINORS
For safety, insurance, and security reasons, no one under the age of 18 is permitted in the expo halls or conference meeting rooms at the event. No childcare services are available onsite.

MEDIA CENTER
Located in Mission City Ballroom M1, the Media Center is open to registered exhibitors and their representatives, as well as members of the press and analysts. You must have a media badge for access. If you would like to set up any meetings please reach out to: pr.ime@informa.com.

SPEAKER CENTER
Located in Mission City Ballroom M1, the Speaker Center is open to registered speakers, as well as members of the DesignCon committees. You must have a speaker badge or be a current committee member for access.

This guide was created on January 10, 2023. Utilize the DesignCon 2023 app for the most up-to-date information on exhibitors, sessions, and networking.

KEYSIGHT

EDUCATION FORUM

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Simulation
USB
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and MORE

February 1

Visit Us in the Great America K Room

Emerging Engineers at DesignCon

DesignCon welcomes engineers of all levels of experience – including those with less than 10 years of professional history. Mark your schedule for DesignCon's first-ever Emerging Engineer Networking Breakfast and twelve 2023 educational sessions led by engineering masters designed for this experience level.

NEW: EMERGING ENGINEER NETWORKING BREAKFAST

Connect with peers looking to expand their professional reach, explore companies and organizations in electronics offering support for those emerging in their careers, and ask questions of established, highly regarded engineers and authors from the DesignCon community while enjoying a continental breakfast and raffle giveaways, including two All Access passes to DesignCon 2024 and gift cards.

Open to all DesignCon attendees, Thursday, February 2, 8:30-10 am.

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UCSC Silicon Valley Extension PROFESSIONAL EDUCATION

The eecosystem Advanced Electronics Engineering Podcast

EDUCATIONAL CONTENT

Highlights include:

- Hands-On PDN Impedance & Calibration Basics, presented by Keysight's Heidi Barnes, Picotest's Steve Sandler, and Northrop Grumman's Benjamin Dannan
- Quick & Easy Dielectric Constant Measurements of Laminate Materials, taught by Eric Bogatin, fellow with Teledyne LeCroy and professor at University of Colorado, Boulder
- Maintaining Manufacturing ROI for Engineering Startups
- And panels like Real-World Deployment of AI/ML in Chip & Board Applications and Test & Measurement for Automotive Standards

SCAN THE QR CODE FOR THE FULL LIST OF SESSIONS

View the conference pages of this guide for more details on these sessions.

WEDNESDAY, FEBRUARY 1, 2023 | BALLROOM B

IEEE Spectrum Emerging Chips & Markets

What will be the technologies driving the next great waves of innovation in semiconductors? Learn about them at this exclusive collaboration between I*EEE Spectrum* and DesignCon, "Emerging Chips & Markets." At this daylong education track, you'll hear from the founders, executives, and researchers at the forefront of translating today's breakthroughs into tomorrow's major industries. You'll gain insights available nowhere else and get firsthand briefings about the key challenges in artificial-intelligence accelerators, wide-bandgap semiconductors, micro-LEDs, quantum computing, and more.

SESSIONS INCLUDE:

- **New Directions in Memory Technology** with **Tom Coughlin**, President of Coughlin Associates; **Debendra Das Sharma**, Senior Fellow and Co-general Manager of Memory and I/O Technologies at Intel; and **David McIntyre**, Director Product Planning and Business Enablement, Device Solutions America at Samsung Semiconductor
- **Hardware Approaches to Qubits** with **Marina Radulaski,** Assistant Professor at University of California, Davis; **David W. Abraham**, Principal Quantum Scientist, IBM T.J. Watson Research Center; and **Guy Ramon**, Physics Department Chair, Santa Clara University
- **Optical Fiber to the Processor** with **Bardia Pezeshki**, CEO at Avicena; **Scott Schube**, Senior Director of Strategic Marketing and Business Development, Data Center Products, Intel; and **Ashkan Seyedi,** Silicon Photonics Product Architect, Nvidia
- **Gallium Nitride vs. Silicon Carbide: Battle of the Wide-Bandgap Semiconductors** with **Umesh Mishra**, Founder and CTO at Transphorm Inc., and **Robert Pilawa-Podgurski**, Professor at University of California, Berkeley
- **Micro-LEDs Rise to the Challenge** with **Kelly Peng**, CEO and Founder at Kura Technologies; **Nikhil Balram**, SVP and GM at Mojo Vision; and **Stephen Yi**, Co-Founder and CTO , Sundiode
- **Revolutionary Number Formats for Machine Learning** with **William Dally**, Chief Scientist at Nvidia, and **John Gustafson**, Chief Scientist at Stealth Startup
- **Emerging AI Accelerator Architectures** with **Manouchehr Rafie,** AI Accelerators Lead at Hewlett Packard Enterprise; **Evgeni Gousev**, Senior Director at Qualcom Technologies; **Andy Hock**, Vice President, Product Management at Cerebras Systems

Scan the QR Code for a full session list with descriptions.

Presented by:

IEEE Spectrum

Open to all conference and expo passholders.

TPC MEMBERS

We would like to thank the volunteers who served on the Technical Program Committee (TPC) for DesignCon 2023. Their contributions as reviewers of the abstracts and papers have made it possible for us to maintain the DesignCon standard of excellence and deliver an outstanding program again this year.

Brice Achkir*, Cisco Fellow/VP Eng., Cisco Systems
Joseph Aday*, Sr. Member of Technical Staff, Lockheed Martin
Maria Agoston*, Principal Engineer, Tektronix
John Andresakis, Director of Business Development, Ohmega/Ticer Technologies
Bruce Archambeault, Retired
Pervez Aziz*, Senior Principal Engineer, Nvidia
Seungyong (Brian) Baek, SI Architect, Apple
Nitin Bhagwath, Principal Technical Product Manager, Cadence
Rula Bakleh*, Principal SI/PI Consultant, Graphcore
Heidi Barnes*, SI/PI Applications Engineer, Keysight Technologies
Josiah Bartlett*, Principal Engineer in Asics and Technology Organization, Tektronix
Wendem Beyene*, Principal Engineer/Manager, Programmable Hardware Engineering, Intel
Luis Boluna, Sr. Application Engineer, Keysight Technologies
David Brunker, Technical Fellow, Molex
Robert Carter*, Vice President of Technology and Business Development, Oak-Mitsui Technologies
Chris Cheng*, Distinguished Technologist, HP Enterprise
David Choe, Principal Applications Engineer, Cadence
Antonio Ciccomancini Scogna*, Signal Integrity and EMC Technologist, Western Digital
Davi Correia, Sr. Principal Application Engineer, Cadence Design Systems
Ben Dannan, Technical Fellow and Staff Digital Engineer, Northrup Grumman
O.J. Danzy, Senior Application Engineer, Keysight Technologies
Jan De Geest, Senior Staff R&D Signal Integrity Engineer, Amphenol
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Vladimir Dmitriev-Zdorov, Principal Engineer, Siemens
Greg Edlund, Senior Engineer, IBM
Jason Ellison*, Sr. Staff Signal Integrity Engineer, Amphenol
Paul Franzon, Cirrus Logic Distinguished Professor, Director of Graduate Programs, NCSU
Sanjeev Gupta*, Optical Network Engineer, Amazon Web Services (AWS)
Sunil Gupta, SIPI Technical Lead, Qualcomm Technologies
Robert Haller*, Sr. Principal Hardware Engineer, Extreme Networks
Gert Havermann, Signal Integrity Engineer, HARTING
Allen F. Horn III*, Research Fellow, Rogers
Rockwell Hsu, Technical Leader, Cisco Systems
Seunghyun Hwang, Principal Engineer, Nvidia
Joungho Kim, Professor, KAIST
Namhoon Kim, Chip Package Design Architect, Google
Akhilesh Kumar, Principal R&D Engineer, Ansys
Beomtaek Lee, Sr. Principal Engineer, Intel
Mike Li*, Fellow, Intel
Zhe Li, Hardware Engineer, Google
Cathy Liu*, Distinguished Engineer, Broadcom
Chris Loberg*, Marketing Manager, Tektronix
Om Mandhana, Staff Services AE, Cadence Design Systems
Henri Maramis, President/CEO, TrackingTheWorld
Marko Marin*, Technical Account Manager, ANSYS
Jon Martens, Fellow, Anritsu
Mehdi Mechaik*, Sr. Signal Integrity Engineer, Amazon Lab126
Ted Mido, Principal R&D Engineer, Synopsys

TPC MEMBERS

Akshay Mohan, EM Technology Lead, Amazon Lab126
Jose Moreira*, Senior Staff Engineer, Advantest
Zhen Mu*, Product Engineering Architect, Cadence Design Systems
Riaz Naseer, Staff Signal Integrity Engineer, Intel
Alfred P. Neves*, Chief Technologist, Wild River Technology
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Pete Pupalaikis, VP, Technology Development, Teledyne LeCroy
Kelvin Qiu, Senior Signal Integrity and Power Integrity Engineer, Google
Fangyi Rao, Master Engineer, Keysight Technologies
Lee Ritchey, President, Speeding Edge
Gerardo Romo-Luevano*, Sr. Staff Engineer/Manager, Qualcomm
Steve Sandler, Managing Director, Picotest
Venkat Satagopan*, Sr. Staff Signal Integrity Engineer, Nvidia
Christian Shuster, Professor, Hamburg University of Technology (TUHH)
Yan Fen Shen, Analog Engineer, Intel
Masashi Shimanouchi, Design Engineer, Intel
Yuriy Shlepnev, President, Simberian
Ben Silva, Analog Engineer, Intel
Bert Simonovich, President, Lamsim Enterprises
Chad Smutzer, Senior Engineer, Mayo Clinic
Mike Steinberger, Consulting Software Engineer, MathWorks
Ransom Stephens*, Consulting Senior Scientist at BitifEye Digital Solutions and Sage at Ransom's Notes
Changyi Su, Staff Design Engineer, AMD
Suresh Subramaniam, Principal Engineer/Architect, AMD
Madhavan Swaminathan, John Pippin Chair Professor in Microsystems Packaging & Emag, Georgia Tech
Donald Telian, Owner/Consultant, SiGuys
Lars Thon*, Consultant, LT Engineering
Thomas To*, Director, AMD
Peter Tomaszewski, Sr. Digital Solutions Engineer, Keysight Technologies
Ambrish Varma*, Sr. Principal Software Engineer, Cadence Design Systems
Harald von Sosen, Principal Engineer, Siemens
Juan Wang, Senior Staff Engineer, AMD
Scott Wedge, Principal Engineer, Siemens EDA
Todd Westerhoff*, Product Marketing Manager, Siemens
Markus Witte, Systems Engineer, Grimme
Randy Wolff, Principal Signal Integrity Engineer, Micron Technology
Hsinho Wu*, Design Engineer, Intel
Ken Wu, Principal MTS, Package and SI/PI Lead, Rivos
Chris Wyland*, Sr. Staff Engineer, Juniper Networks
Kai Xiao, Principal Engineer, Intel
Mobashar Yazdani*, Strategic Semiconductor Manager, Google
Iliya Zamek, Architect, Technical Manager, HCL America
Geoffrey Zhang, Distinguished Engineer and Supervisor, AMD
Pavel Zivny, Domain Expert, Tektronix

*2023 track co-chair

DesignCon® 2023

WHERE THE CHIP MEETS THE BOARD

KEYNOTES Open to All Attendees

Aydin Aysu

Assistant Professor and Head of the Hardware Cybersecurity Research Lab (HECTOR) in the Electrical & Computer Engineering Department of North Carolina University

Post-Quantum Cryptography: The Next Decade of Cryptographic Hardware Design

Tuesday, January 31, 2023
11:45am-12:30pm
Elizabeth A. Hangs Theater, 2nd Floor

Existing cryptographic standard algorithms cannot move to the quantum computing era because quantum computers are proven to break them. Advances in quantum computing technology are creating concerns for such a practical break. To address this issue, we must completely change the cryptography infrastructure in the next decade and use new algorithms in secure communication and access control protocols.

Devin Billings

Associate Director of Electrical Research and Development at Boston Dynamics

Enabling Autonomous Robotics Through Electrical Engineering

Wednesday, February 1, 2023
10:00-11:00am
Elizabeth A. Hangs Theater, 2nd Floor

Building machines that can approximate the mobility, dexterity, and agility of people and animals is a grand challenge. Through a combination of advancements in robotic control, AI, and many forms of hardware component technology, we may be on the precipice of a proliferation of massively scalable new robotic automation opportunities. But these kinds of robots represent quite complex design challenges in electrical system design, necessitating technology that encompasses a huge range of subject matter within the electrical engineering discipline.

This keynote is preceded by the 2022 Best Paper Award presentations.

Ben Gu

Vice President Research and Development, Multiphysics System Analysis Business Unit at Cadence Design Systems

The Intelligence to Design Intelligent Machines

Thursday, February 2, 2023
10:00-11:00am
Elizabeth A. Hangs Theater, 2nd Floor

Electronics design is undergoing a revolution as semiconductors are used in more and more market applications. Each has its unique data and workload and requires customized compute and analytics architectures. Advanced semiconductors are implemented in the latest process nodes, in the most complex 3D-ICs, to achieve top performance with more operational flexibility. When the scope is expanded to the full system, complexity further exceeds the traditional siloed engineering teams and methodology. AI is showing promise for addressing the growing complexity, but not all problems are equal.

This keynote is preceded by the Engineer of the Year Award presentation.

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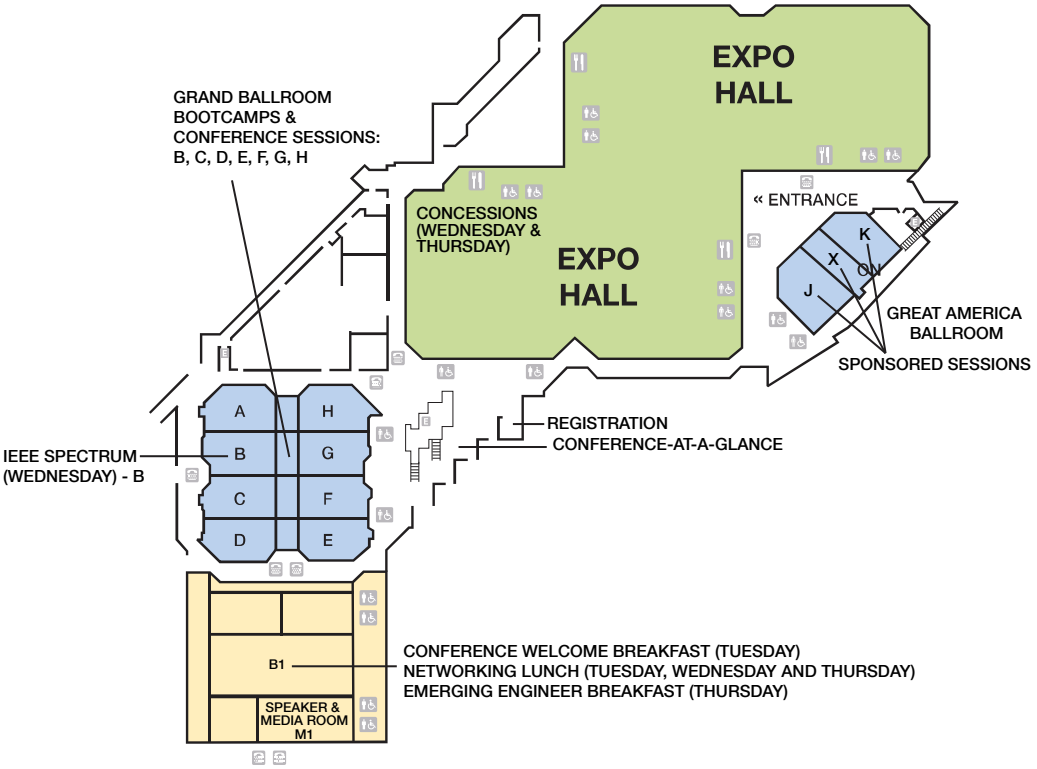
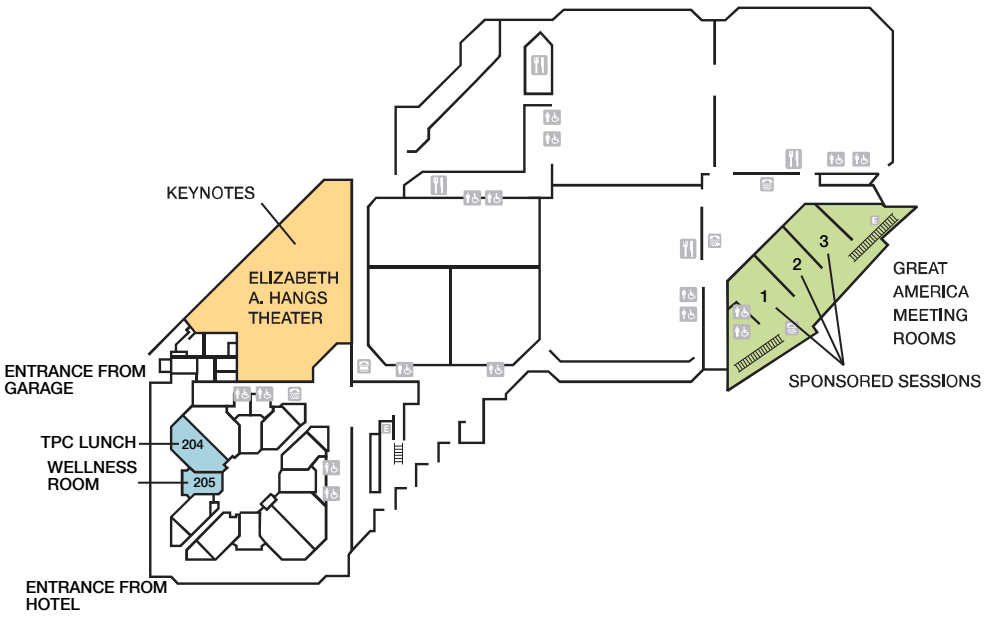
CONFERENCE MAP

FIRST FLOOR



SECOND FLOOR



SESSIONS – TUESDAY, JANUARY 31

8:00 AM – 9:00 AM

Welcome Breakfast
2-Day Pass, All Access Pass — Mission City Ballroom B1

9:00 AM – 4:30 PM

Boot Camp – Memory Design Fundamentals: Next-Generation Memory Systems
All Access Pass — Ballroom GH

9:00 AM – 11:30 AM

Tutorial – Bird's-Eye Viewing 200+Gbps per Lane & Beyond with Various Signal-to-Noise Ratio Metrics
All Access Pass — Ballroom F

Tutorial – Measuring PSNR/PSRR/PSMR to Meet QSFP/OSFP High-Speed Requirements
All Access Pass — Ballroom E

Tutorial – Quantum Computer (Superconductor Qubits) Hardware Design Guidelines
All Access Pass — Ballroom D

11:45 AM –1 2:30 PM

Keynote – Post-Quantum Cryptography: The Next Decade of Cryptographic Hardware Design
2-Day Pass, All Access Pass, Expo Pass — Elizabeth A. Hangs Theater

12:30 PM – 2:30 PM

Conference Networking Lunch
2-Day Pass, All Access Pass — Mission City Ballroom B1

2:00 PM – 4:30 PM

Tutorial – Design & Verification for High-Speed I/Os at 10 to 112 & 224 Gbps with Jitter, Signal Integrity, & Power Optimized
All Access Pass — Ballroom F

Tutorial – Machine Learning for Embedded Developers
All Access Pass — Ballroom E

Tutorial – Stackups: The Design Within the Design
All Access Pass — Ballroom D

Tutorial – PCB Design Techniques to Improve ESD Robustness
All Access Pass — Ballroom C

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise, BER & Channel Imperfections
9. High-Speed Signal Processing, Modulation, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

- D Drive World — Advanced Automotive
- IEEE Spectrum Emerging Chips and Markets
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- General Event
- Special Event
- Sponsored Sessions

Conference Schedule continued on page 20.

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DesignNews

As official media partner of DesignCon, *Design News* serves the brightest minds looking to engineer the technology of tomorrow.

We Inspire Innovation.

Design News media, educational, virtual, and live-event content explores sectors such as electronics, software and sensors, IoT, batteries, AI, AR/VR, smart manufacturing, robotics and cobots, next-generation automotive and aerospace/defense, materials, energy design implementation, and much more — **to ensure that today's engineering accomplishments bring forth tomorrow's tech reality.**

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We'd love to hear from you. Get in touch:

Daphne Allen, Editor-In-Chief

daphne.allen@informa.com

www.designnews.com

SESSIONS – TUESDAY, JANUARY 31

4:45 PM – 6:00 PM

Panel – Enabling Next Generation Co-Packaging Solutions
2-Day Pass, All Access Pass, Expo Pass — Ballroom D

Panel – PCIe 6.0: Challenges of Achieving 64GT/s with PAM4 in Lossy, HVM Channels
2-Day Pass, All Access Pass, Expo Pass — Ballroom F

Panel – Real-World Deployment of AI/ML in Chip & Board Applications
2-Day Pass,All Access Pass,Expo Pass — Ballroom C

Panel – The Case of the Closing Eyes: Bridging FEC to Signal Integrity
2-Day Pass, All Access Pass, Expo Pass — Ballroom GH

6:00 PM – 8:00 PM

Welcome Reception
Open to all — Santa Clara Ballroom, Hyatt Regency Santa Clara

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TRACKS AND LEGEND

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1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
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3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
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10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
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13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

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- IEEE Spectrum Emerging Chips and Markets
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- General Event
- Special Event
- Sponsored Sessions

Conference Schedule continued on page 22.

SESSIONS – WEDNESDAY, FEBRUARY 1

8:00 AM – 8:45 AM

A Novel Simulation Flow for DDR5 Systems with Clocked Receivers
2-Day Pass, All Access Pass — Ballroom G

Enabling Industry's First Beyond 8.5Gbps/pin LPDDR5X PHY Using Rx Offset Calibration Scheme & Robust Training Method
2-Day Pass, All Access Pass — Ballroom D

High-Speed Loopback Applications by Utilizing a Differential DPDT MEMS Switch
2-Day Pass, All Access Pass — Ballroom E

Next Generation 224 Gbps-PAM4 Chip-to-Module Channel Design, Link Simulation, & Analysis
2-Day Pass, All Access Pass — Ballroom H

Towards 106 GBaud: Analysis of Latest 53 GBaud DUTs Informs the Improvements of Methodology
2-Day Pass, All Access Pass — Ballroom F

Overview of PCB Fabrication Influences on RF Performance for Millimeter-Wave Radar
2-Day Pass, All Access Pass — Ballroom C

New Directions in Memory Technology
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

Technologies That Will Shape The Future Of The Data Center
2-Day Pass, All Access Pass, Expo Pass — Great America 1

8:00 AM – 8:40 AM

In-Situ De-Embedding
2-Day Pass, All Access Pass, Expo Pass — Great America 2

Advanced Testing Challenges at 32GBaud PAM4 with PCIe 6.0
2-Day Pass, All Access Pass, Expo Pass — Great America K

8:55 AM – 9:35 AM

Advanced Jittter Transfer Measurements for PLL Characterization
2-Day Pass, All Access Pass, Expo Pass — Great America K

9:00 AM – 9:45 AM

MIPI CPHY Modeling, Measurement & Correlation for AR/VR Devices
2-Day Pass, All Access Pass — Ballroom E

How to Design Secured Power Delivery Network of Cryptographic Devices: Challenges, Evaluation Methods, & Solutions
2-Day Pass, All Access Pass — Ballroom D

One-Phase Immersion Cooling Liquids Characterization
2-Day Pass, All Access Pass — Ballroom H

Simulation & Analysis of Electrical/Optical Communication Links Using Free Software
2-Day Pass, All Access Pass — Ballroom G

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise, BER & Channel Imperfections
9. High-Speed Signal Processing, Modulation, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

D. Drive World — Advanced Automotive

IEEE Spectrum Emerging Chips and Markets

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General Event

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Conference Schedule continued on page 24.

SESSIONS – WEDNESDAY, FEBRUARY 1

9:00 AM – 9:45 AM

VRM Modeling & Stability Analysis for Power Integrity Engineers
2-Day Pass, All Access Pass — Ballroom F

Wiring the Future of Mobility
2-Day Pass, All Access Pass — Ballroom C

Hardware Approaches to Qubits
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

9:00 AM – 9:40 AM

Successful PCIe Interconnect Guidelines for 8, 16, and 32 GT/s
2-Day Pass, All Access Pass, Expo Pass — Great America 2

9:00 AM – 9:45 AM

Choosing The Right High-Performance Memory Solution
2-Day Pass, All Access Pass, Expo Pass — Great America 1

Interconnect Trends & Guidance for Automotive High-Speed Applications
2-Day Pass, All Access Pass, Expo Pass — Great America J

10:00 AM – 11:00 AM

Keynote – Enabling Autonomous Robotics Through Electrical Engineering
2-Day Pass, All Access Pass, Expo Pass — Elizabeth A. Hangs Theater

11:10 AM – 11:50 AM

112 Gbps PAM4 Front Panel Connectivity - Real World Implementation & Correlation
2-Day Pass, All Access Pass, Expo Pass — Great America 2

Next Gen Development in USB4 Version 2.0
2-Day Pass, All Access Pass, Expo Pass — Great America K

11:15 AM – 12:00 PM

A New Power Integrity Requirement to Supplement Target Impedance: Quantifying PDN Impedance Flatness from Sandler NISM
2-Day Pass, All Access Pass — Ballroom G

End-to-End Security Features Protecting Mission-Critical Data for CXL Based Platforms
2-Day Pass, All Access Pass — Ballroom E

Best Practices for A Converged High-Speed Channel Design for Cloud Servers in Both Air-Cooling & Immersion-Cooling
2-Day Pass,All Access Pass — Ballroom F

Statistical BER Analysis of Concatenated FEC in Multi-Part Links
2-Day Pass, All Access Pass — Ballroom D

Package & IC Aware PCB PDN Design by Optimizing Decoupling Capacitors While Evaluating PDN Voltage Ripple Noise
2-Day Pass, All Access Pass — Ballroom H

TRACKS AND LEGEND

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- Chiphead Theater Presentation
- General Event
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- Sponsored Sessions

Conference Schedule continued on page 26.

SESSIONS – WEDNESDAY, FEBRUARY 1

11:15 AM – 12:00 PM

More Relevant Than Ever: Safety & Security for Automotive Sensing Systems
2-Day Pass, All Access Pass — Ballroom C

Optical Fiber to the Processor
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

11:15 AM – 12:15 PM

Panel – Deploying ML in EDA Context: Operation & Organization
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

11:15 AM – 12:00 PM

Panel: Automotive IP Solutions For The Software-Defined Vehicle
2-Day Pass, All Access Pass, Expo Pass — Great America 1

OCP ORv3 Rack & Power Distribution Overview
2-Day Pass, All Access Pass, Expo Pass — Great America J

11:55 AM – 12:35 PM

Intuitive Simulation & Measurement Workflow for Hardware Engineers
2-Day Pass, All Access Pass, Expo Pass — Great America K

12:10 PM – 12:50 PM

Mastering Phase Noise/Jitter Measurements
2-Day Pass, All Access Pass, Expo Pass — Great America 2

12:15 PM – 1:00 PM

Data-Efficient Supervised Machine Learning Technique for Practical PCB Noise Decoupling
2-Day Pass, All Access Pass — Ballroom D

Finite Element Modelling of Copper Foil Loss from AFM Measurements
2-Day Pass, All Access Pass — Ballroom F

Mm-Wave Communication Over Dielectric Waveguides: System Design & Applications
2-Day Pass, All Access Pass — Ballroom H

The IC-level Conducted Emission Measurement & Simulation Analysis for an Automotive DRAM
2-Day Pass, All Access Pass — Ballroom G

Optimal Design & Swift Workflow for Multi-Layer Structures
2-Day Pass, All Access Pass — Ballroom E

Designing a Configurable ECU with Python
2-Day Pass, All Access Pass — Ballroom C

Gallium Nitride vs. Silicon Carbide: Battle of the Wide-Bandgap Semiconductors
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

Security IP Solutions For A World Of IoT Devices
2-Day Pass, All Access Pass, Expo Pass — Great America 1

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SPEAKER

PHASES OF THE IC DEVELOPMENT CYCLE

THURSDAY, FEBRUARY 2 | 11:15 AM-12:00 PM | CHIPHEAD THEATER, SANTA CLARA CONVENTION CENTER

IBRAHIM DELIBALTA | Ph.D., Sr. Director of SoC Design at Intel Corporation | UCSC Extension Instructor
Introduction to VLSI and ASIC Design | Spring 2023

ucsc-extension.edu

SESSIONS – WEDNESDAY, FEBRUARY 1

12:30 PM – 1:30 PM

Panel – Advanced Technologies for Line Card Design
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

12:30 PM – 2:30 PM

Conference Networking Lunch
2-Day Pass, All Access Pass — Mission City Ballroom B1

1:45 PM – 2:30 PM

Maintaining Manufacturing ROI for Engineering Startups
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

2:00 PM – 2:45 PM

A Novel Approach to 224 Gb/s Reference Receiver Design Using Raised Cosine Response for Noise Mitigation
2-Day Pass, All Access Pass — Ballroom G

A Novel Crosstalk Reduction Technique for DDR5 Server Application
2-Day Pass, All Access Pass — Ballroom E

An Innovative CPU Pin-Field Routing for Signal Integrity Optimization
2-Day Pass, All Access Pass — Ballroom D

2:00 PM – 2:45 PM

MIMO Crosstalk Cancelation Technique in Serial Electrical Links
2-Day Pass, All Access Pass — Ballroom H

Measurement Bandwidth & Its Impact on Accuracy
2-Day Pass, All Access Pass — Ballroom F

4K eDP Vehicular Display Micro-Coax Cable Designs
2-Day Pass, All Access Pass — Ballroom C

Micro-LEDs Rise to the Challenge
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

2:00 PM – 2:40 PM

Far-End Crosstalk In High-Speed PCB Channels
2-Day Pass, All Access Pass, Expo Pass — Great America 2

2:00 PM – 2:45 PM

Accelerating Data Interconnects With PCI Express 6.0 Interface IP
2-Day Pass, All Access Pass, Expo Pass — Great America 1

224G Connector Solution
2-Day Pass, All Access Pass, Expo Pass — Great America J

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SESSIONS – WEDNESDAY, FEBRUARY 1

2:40 PM – 3:20 PM

Physical Layer Validation Challenges of Characterizing 100/200 Gbps/lane Designs
2-Day Pass, All Access Pass, Expo Pass — Great America K

2:45 PM – 3:00 PM

Accurate SI Analysis for PCIe Gen5 Signaling with PCB & Connector Merged Structure up to 50GHz
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

3:00 PM – 3:40 PM

Dielectric Permittivity Extraction For Inhomogeneous Dielectric Layers Based On Delta-L & Extended Unterminated Line (EUL) Measurements
2-Day Pass, All Access Pass, Expo Pass — Great America 2

3:00 PM – 3:45 PM

Comprehensive Statistical Analysis of SERDES Links Considering DFE Error Propagation
2-Day Pass, All Access Pass — Ballroom G

ML-Based AMOP Framework for On-chip Test Sequence Thermal Optimization
2-Day Pass, All Access Pass — Ballroom H

PCIe 6.0 (PAM4) Signal Integrity Challenges in Immersion-Cooling Datacenters
2-Day Pass, All Access Pass — Ballroom D

3:00 PM – 3:45 PM

PCIe Gen5, Signal Integrity Implementation Issues & Solutions
2-Day Pass, All Access Pass — Ballroom E

The Influence of EM Field Solver Numerical Solution Space on Measurement Correlation to 50GHz & Beyond
2-Day Pass, All Access Pass — Ballroom F

Pushing the Boundaries of Automotive Connectivity
2-Day Pass, All Access Pass — Ballroom C

Revolutionary Number Formats for Machine Learning
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

3:00 PM – 3:45 PM

CXL Advances Data Center Performance With Memory Tiering Architecture
2-Day Pass, All Access Pass, Expo Pass — Great America 1

3:15 PM – 4:00 PM

Panel – Will AI Ever Replace Engineers?
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

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SESSIONS – WEDNESDAY, FEBRUARY 1

3:30 PM – 4:10 PM

IBIS/IBIS-AMI for SerDes and Memory Applications
2-Day Pass, All Access Pass, Expo Pass — Great America K

4:00 PM – 4:40 PM

Improve Power Integrity With Pre-Layout Decoupling Solutions
2-Day Pass, All Access Pass, Expo Pass — Great America 2

4:00 PM – 5:15 PM

Panel – Compute Express Link (CXL) 3.0: Enabling New Usage Models in Composable Disaggregated Infrastructure
2-Day Pass, All Access Pass, Expo Pass — Ballroom D

Panel – Enabling Next Generation Architectures: 224 Gbps Electrical Interfaces
2-Day Pass, All Access Pass, Expo Pass — Ballroom G

Panel – What Users Need from Power Integrity Simulators
2-Day Pass, All Access Pass, Expo Pass — Ballroom F

Panel – Revolutionizing In-Vehicle PHY Channel Characterization (>10Gbps): Is Simulation the Solution?
2-Day Pass, All Access Pass, Expo Pass — Ballroom C

Emerging AI Accelerator Architectures
2-Day Pass, All Access Pass, Expo Pass — Ballroom B

4:15 PM – 5:00 PM

Micro-coax Cable Transfer Performance of High-speed Differential Signals
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

4:20 PM – 5:00 PM

Advanced Power Integrity Simulation & Measurement Methods
2-Day Pass, All Access Pass, Expo Pass — Great America K

5:00 PM – 6:00 PM

Booth Bar Crawl
2-Day Pass, All Access Pass, Expo Pass — Expo Hall

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SESSIONS – THURSDAY, FEBRUARY 2

8:00 AM – 8:45 AM

Analytical Models for FEC Symbol Error Distribution of DFE Propagation with Precoding and EoBD
2-Day Pass, All Access Pass — Ballroom G

Effect of Intra-Pair Skew on Copper Cable Assembly Link Performance
2-Day Pass, All Access Pass — Ballroom E

Extremely Fast Dynamic Link Equalization for PCIe Based on Imitation Learning
2-Day Pass, All Access Pass — Ballroom D

Impact Evaluation of Fiber-Weave Effect Induced Delay Uncertainty in DDR Data Links on DDR5 & Towards DDR6
2-Day Pass, All Access Pass — Ballroom F

Noise in Traffic: Signal Emulation for Automotive Apps
2-Day Pass, All Access Pass — Ballroom H

Centralized Storage for Next Generation Vehicles: New Standards & Future Roadmaps
2-Day Pass, All Access Pass — Ballroom C

How to Measure Jitter Induced by Power Distribution Network (PDN) Noise
2-Day Pass, All Access Pass, Expo Pass — Great America K

Addressing Package/PCB Thermal Challenges by Extending Your Power Integrity Analysis Methodology
2-Day Pass, All Access Pass, Expo Pass — Great America J

8:30 AM – 10:00 AM

Emerging Engineer Breakfast
2-Day Pass, All Access Pass, Expo Pass — Mission City Ballroom B1

9:00 AM – 9:45 AM

3D Connection Artifacts in PDN Measurements
2-Day Pass, All Access Pass — Ballroom G

A Case Study of Soft Information & Decoding Concatenated Codes for Optical Applications
2-Day Pass, All Access Pass — Ballroom D

Cost Optimized PCB Design for DDR5
2-Day Pass, All Access Pass — Ballroom E

Managing Differential Via Crosstalk & Ground Via Placement for 40+ Gbps Signaling
2-Day Pass, All Access Pass — Ballroom F

System Design Challenges with 5G & mmwWave Integration
2-Day Pass, All Access Pass — Ballroom H

Beyond 10Gbps Automotive Ethernet: Is Optical Connectivity the Solution?
2-Day Pass, All Access Pass — Ballroom C

USB4® Version 2.0 Transmitter (Tx) & Receiver (Rx) Electrical Compliance Test Update
2-Day Pass, All Access Pass, Expo Pass — Great America K

PowerTree-based PDN Analysis, Correlation & Signoff for AR Systems
2-Day Pass, All Access Pass, Expo Pass — Great America J

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SESSIONS – THURSDAY, FEBRUARY 2

10:00 AM – 11:00 AM

Keynote – The Intelligence to Design Intelligent Machines
2-Day Pass, All Access Pass, Expo Pass
Elizabeth A. Hangs Theater

11:15 AM – 12:00 PM

Accuracy & Challenges of PAM4 Jitter & Noise Measurements for >100Gbps Serial Links
2-Day Pass, All Access Pass
Ballroom F

Design of a SI/PI Optimized PCIe 6 Platform to Enable PCIe 7
2-Day Pass, All Access Pass
Ballroom D

Cascaded vs End-to-End Multi-Pin Interconnect Simulation Models
2-Day Pass, All Access Pass
Ballroom H

Data-Driven PAM4 SerDes Modeling & Generative Adversarial Network
2-Day Pass, All Access Pass
Ballroom G

SPICE-Compatible Behavior Model of Multiphase Voltage Regulator Module for End-to-End Power Integrity Simulation
2-Day Pass, All Access Pass
Ballroom E

Feasibility of End-to-End Ethernet for Sensor & Display Connectivity in Automotive Applications
2-Day Pass, All Access Pass
Ballroom C

11:15 AM – 12:00 PM

How To Debug USB4® PHY-Logic & Sideband Links
2-Day Pass, All Access Pass, Expo Pass
Great America K

When Chips Become 3D Systems – The Challenges of Designing Multi-Chiplet Packages
2-Day Pass, All Access Pass, Expo Pass
Great America J

Phases of the IC Development Cycle
2-Day Pass, All Access Pass, Expo Pass
Chiphead Theater

12:15 PM – 1:00 PM

Evaluating 224G SI Performance of Discrete DC Blocking Capacitors on Optical Modules & Systems
2-Day Pass, All Access Pass
Ballroom E

COM Based IBIS-AMI Correlation Including Actual System & Circuit Behaviors for 106/112Gb/s
2-Day Pass, All Access Pass
Ballroom D

Designing the Best Reference Transmitter for Serdes Testing: AWG vs BER
2-Day Pass, All Access Pass
Ballroom F

NextGen Copper Foils for High-Speed Digital & Radio Frequency Applications
2-Day Pass, All Access Pass
Ballroom G

Scalable Capacitor ESL Curve Fitting for Various Stack-ups
2-Day Pass, All Access Pass
Ballroom H

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SESSIONS – THURSDAY, FEBRUARY 2

12:15 PM – 1:00 PM

Multi-Sensor Annotation & Calibration is the Key Unlocking ADAS Applications
2-Day Pass, All Access Pass — Ballroom C

Chipheads: Hands-On PDN Impedance & Calibration Basics
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

Cross-layer Analysis & Debug of PCI Express® Power Management & Link Training
2-Day Pass, All Access Pass, Expo Pass — Great America K

Encore Presentation: Optimal Design & Swift Workflow for Multi-Layer Structures
2-Day Pass, All Access Pass, Expo Pass — Great America J

12:30 PM – 2:30 PM

Conference Networking Lunch
2-Day Pass, All Access Pass — Mission City Ballroom B1

1:15 PM – 2:00 PM

Quick & Easy Dielectric Constant Measurements of Laminate Materials
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

2:00 PM – 2:45 PM

3D EM Full Wave Analysis & Optimization for Source Synchronous Interconnect in Heterogeneous Integration Architecture
2-Day Pass, All Access Pass — Ballroom G

Distributed-Physical-Based Transmission-Line Model of PCIe5 Connector for SI Fast Diagnosis
2-Day Pass, All Access Pass — Ballroom D

High Speed System Architecture Design of DCN Core Switch
2-Day Pass, All Access Pass — Ballroom E

IP/PHY & Testing are Critical for USB4 Version 2.0
2-Day Pass, All Access Pass — Ballroom H

Rigorous Correlation Methodology for PCIe Gen5 & Gen6 DSP Based IBIS-AMI Models
2-Day Pass, All Access Pass — Ballroom F

The Billion Dollar Mistake
2-Day Pass, All Access Pass — Ballroom C

Understanding & Implementing PCI Express® 6.0 Receiver Test Requirements
2-Day Pass, All Access Pass, Expo Pass — Great America K

Envisioning the Future of Power Integrity Through the Eyes of Experience
2-Day Pass, All Access Pass, Expo Pass — Great America J

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SESSIONS – THURSDAY, FEBRUARY 2

2:15 PM – 3:00 PM

Backplanes, Speed Gains & Architectural Autonomy: Evolution of Copper Interconnects
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

3:00 PM – 3:45 PM

A Simple TDR Technique to Measure the Dielectric Constant of Any Layer in a Multi-Layer Printed Circuit Board
2-Day Pass, All Access Pass — Ballroom E

An EMI Reduction Modeling Approach of PCB & Shielding Enclosures Using the Lua-based Automation
2-Day Pass, All Access Pass — Ballroom H

IBIS-AMI Modeling & Simulation for PAM3 Signaling in USB4 Gen4 Systems
2-Day Pass, All Access Pass — Ballroom G

Learning Beyond Low-Quality Data Distribution: An Application to Optimal Decap Placement
2-Day Pass, All Access Pass — Ballroom F

3:00 PM – 3:45 PM

Measurement-Based Bias Voltage, Temperature, & Light Intensity Effect on the Through-silicon Vias (TSVs)
2-Day Pass, All Access Pass — Ballroom D

Supply & Demand Trends in Automotive ICs
2-Day Pass, All Access Pass — Ballroom C

PCI Express® 6.0 Transmitter Electrical Test Overview
2-Day Pass, All Access Pass, Expo Pass — Great America K

Optimizing 3D-IC Power Delivery with Pre-Route System-Level Simulation
2-Day Pass, All Access Pass, Expo Pass — Great America J

3:15 PM – 4:00 PM

Limits of High speed Connector & Cable Technology, Part 2
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

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6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise, BER & Channel Imperfections
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10. Power Integrity in Power Distribution Networks
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12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
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D. Drive World — Advanced Automotive

IEEE Spectrum Emerging Chips and Markets

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Conference Schedule continued on page 42.

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SESSIONS – THURSDAY, FEBRUARY 2

4:00 PM – 5:15 PM

Panel – FEC for Next Generation 800G/1.6T Ethernet Systems
2-Day Pass, All Access Pass, Expo Pass — Ballroom G

Panel – PCI Express Specification: A High-Bandwidth, Low-Latency Interface for the Compute Continuum
2-Day Pass, All Access Pass, Expo Pass — Ballroom F

Panel – Photonics Future: Vision, Challenges, and the Path to Infinity & Beyond!
2-Day Pass, All Access Pass, Expo Pass — Ballroom D

4:00 PM – 5:15 PM

Panel – Test on Wheels: Test & Measurement for Automotive Standards
2-Day Pass, All Access Pass, Expo Pass — Ballroom C

A Simple Method For De-embedding Fixtures Using S-parameter Measurements
2-Day Pass, All Access Pass, Expo Pass — Great America K

PCIe Rising: The Journey to 64Gb/s and 128Gb/s
2-Day Pass, All Access Pass, Expo Pass — Great America J

4:15 PM – 5:00 PM

Panel - Overcoming Career Challenges for Millenials
2-Day Pass, All Access Pass, Expo Pass — Chiphead Theater

5:00 PM – 6:00 PM

Booth Bar Crawl
2-Day Pass, All Access Pass, Expo Pass — Expo Hall

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14. Machine Learning for Microelectronics, Signaling & System Design

- D Drive World — Advanced Automotive
- IEEE Spectrum Emerging Chips and Markets
- Best Paper Awards Finalist
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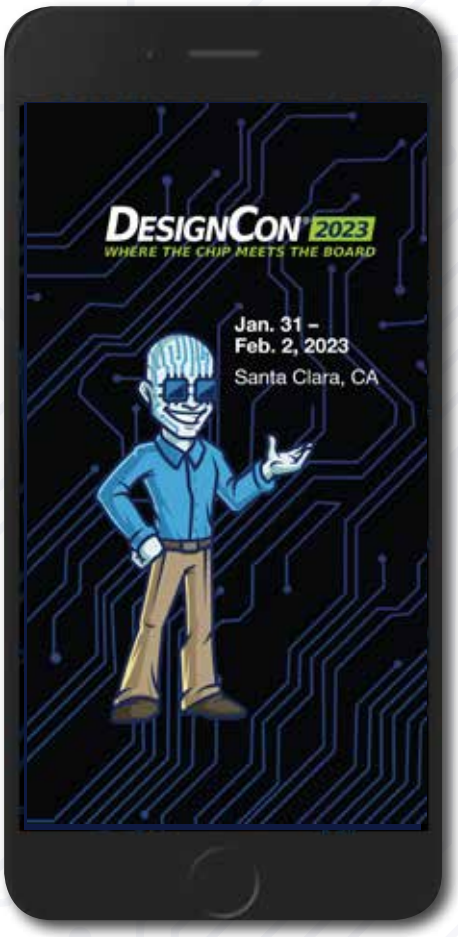

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Ansys	748
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EXHIBIT HALL FLOOR MAP

EXHIBIT HOURS:

Wednesday, February 1
11:00 AM - 6:00 PM

Thursday, February 2
11:00 AM - 6:00 PM

- Wednesday Product Showcase Locations
- Thursday Product Showcase Locations
- Wednesday Booth Bar Crawl
- Thursday Booth Bar Crawl

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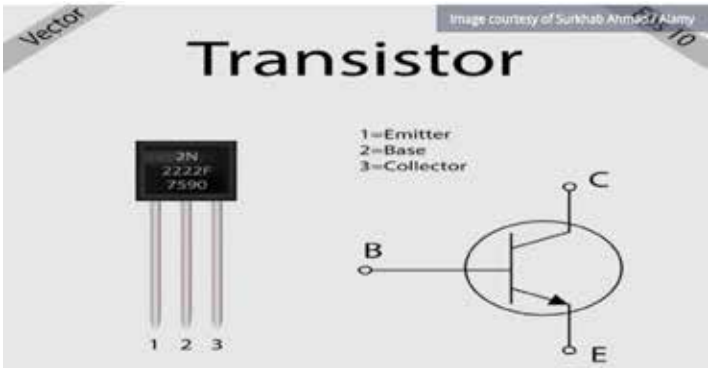
Key Milestones in the Transistor's Evolution

Here are some significant dates in the evolution of the transistor, which turned 75 in December 2022.

By Spencer Chin, Senior Editor, *Design News*



The transistor, invented in 1947, is key to many electronic devices we use on a daily basis.
Image courtesy of Surkhab Ahmad/Alamy

The first transistor was successfully demonstrated at Bell Laboratories in Murray Hill, New Jersey, in 1947. This three-terminal device has spawned many of the electronics devices that make possible many of the products we take for granted today. From the transistor came MOSFETs in its various incarnations, integrated circuits, and microprocessors.

While early transistors produced humble inventions such as transistor radios, subsequent improvements in transistor technology later produced calculators, personal computers, and power electronics devices.

What follows below is a summary of the more significant developments in the transistor's rich history. Design News thanks Wikipedia for the information in this story.

EARLY HISTORY

According to Wikipedia, the first patent for the field-effect transistor was filed by Austrian-Hungarian physicist Julius Edgar Lilienfeld on October 25, 1925, but as he published no research articles about his devices, his work was ignored by industry.

Bell Lab's transistor development efforts stemmed from war-time efforts to produce highly pure germanium crystal mixer diodes, used in radar units as a frequency mixer element in microwave radar receivers. After World War II, Bell scientists John Bardeen, William Shockley, and Walter Brattain started work on a triode-like semiconductor device. The trick turned out to be producing consistent electron flow between the device's emitter and collector, which was made possible by placing the emitter and collector leads very close together with the control lead at the base of the crystal.

A Purdue University graduate student, who joined the research effort, noted that when voltage was applied, there was no resistance, which gave birth to the idea of minority carrier injection.

Continued on page 49.

Product Showcase

Don’t miss this series of LIVE demos taking place on the DesignCon show floor.

WEDNESDAY, FEBRUARY 1, 2023

TIME	COMPANY	BOOTH
1:30 PM	Tektronix	727
2:00 pm	XPEEDIC	633
2:30 pm	molex	739
3:00 pm	samtec	939
3:30 pm	ROHDE&SCHWARZ Make ideas real	1049
4:30 pm	Rosenberger	1047

THURSDAY, FEBRUARY 2, 2023

TIME	COMPANY	BOOTH
4:30 pm	Rosenberger	1047

DECEMBER 1947: FIRST WORKING TRANSISTOR

Armed with this knowledge, the Bell scientists went through several starts and stops before finally building the first working transistor on December 16, 1947. The point-contact transistor features two closely spaced gold contacts joined by a small piece of germanium.

Barden, Shockley, and Brattain won a Noble Prize in Physics for their efforts.

Bell scientists (left to right) John Bardeen, William Shockley and Walter Brattain, who invented the transistor in 1947.
Image courtesy of PBH Images/Alamy

1954: MOVING TO SILICON

While the first transistor used germanium, this material was not a practical long-term solution because of its limited operating temperature range and difficulties in purifying the compound. A Bell Labs team led by Morris Tanenbaum developed the first working silicon transistor on January 16, 1954. A similar device was developed by Gordon Teal of Texas Instruments a few months later.

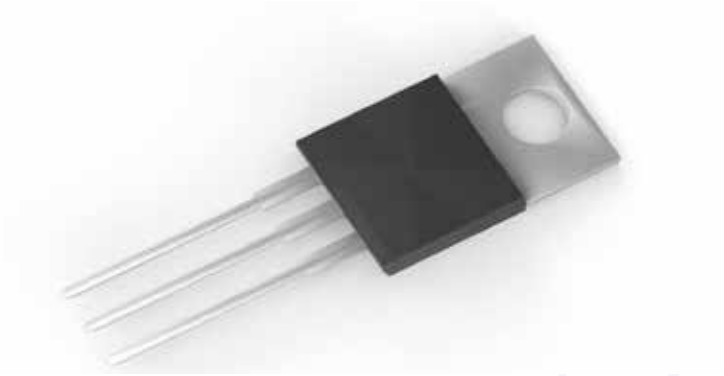
In 1955, Bell Lab scientists discovered the passivating effect of oxidation on the semiconductor surface. The surface passivation method is a key milestone for transistors as it later made possible the mass production of ICs.

1959: PLANAR PROCESS AND MOSFET

The successful demonstration of silicon oxide's passivation of a silicon surface, first by Mohamed Atalla at Bell Labs and Jean Hoerni of Fairchild led to the planar process, which made the mass production of silicon ICs possible.

Also in 1959, the first MOSFET was produced. The metal–oxide–semiconductor field-effect transistor (MOSFET) was invented by Atalla and Dawon Kahng at Bell Labs. They fabricated the device in November 1959 and presented it as the "silicon-silicon dioxide field induced surface device" in early 1960. With its high scalability, and much lower power consumption and higher density than bipolar junction transistors, the MOSFET made it possible to build high-density integrated circuits (ICs) allowing the integration of more than 10,000 transistors in a single IC.

Compared to bipolar transistors, MOSFETS consume no current except when switching states and they have faster switching speed.



The development of the MOSFET in 1959 was a key step in the transistor's evolution. Image courtesy of Zoonar Gmblt/Alamy

1963: CMOS

CMOS (complementary MOS) was invented by Chih-Tang Sah and Frank Wanlass at Fairchild Semiconductor, and in February 1963 they published the invention in a research paper. CMOS technology would prove instrumental in the development of integrated circuits (ICs), including microprocessors, microcontrollers, and memory chips.

Continued on page 50.

1967: FLOATING GATE TRANSISTOR

The first report of a FGMOS was made by Dawon Kahng and Simon Min Sze at Bell Labs, and dates from 1967. The floating-gate MOSFET (FGMOS), also known as a floating-gate MOS transistor or floating-gate transistor, is a type of metal–oxide–semiconductor field-effect transistor (MOSFET) where the gate is electrically isolated, creating a floating node in direct current, and a number of secondary gates or inputs are deposited above the floating gate (FG) and are electrically isolated from it. These inputs are only capacitively connected to the FG.

Initial applications of FGMOS were digital semiconductor memory, to store nonvolatile data in EPROM, EEPROM and flash memory.

1967: SELF-ALIGNED GATE

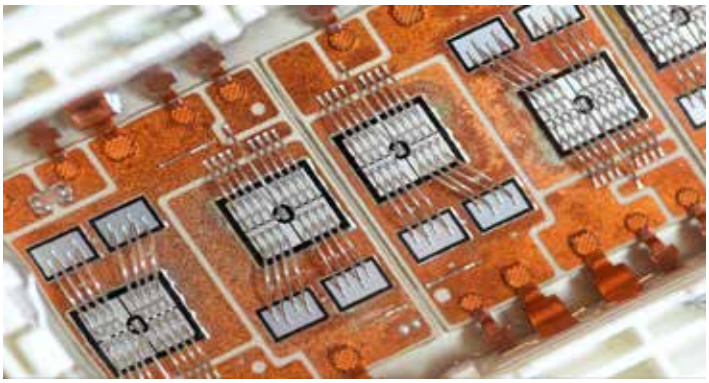
The self-aligned gate (silicon-gate) MOSFET transistor was invented by Robert Kerwin, Donald Klein and John Sarace at Bell Labs in 1967. Fairchild Semiconductor researchers Federico Faggin and Tom Klein later used self-aligned gate MOSFETs to develop the first silicon-gate MOS integrated circuit.

1979: INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

The basic IGBT mode of operation, where a PNP transistor is driven by a MOSFET, was first proposed by K. Yamagami and Y. Akagiri of Mitsubishi Electric in the Japanese patent S47-21739, filed in 1968.

Following the commercialization of power MOSFETs in the 1970s, B. Jayant Baliga submitted a patent disclosure at General Electric (GE) in 1977 describing a power semiconductor device with the IGBT mode of operation, including the MOS gating of thyristors, a four-layer VMOS (V-groove MOSFET) structure, and the use of MOS-gated structures to control a four-layer semiconductor device. He began fabricating the IGBT device with the assistance of Margaret Lazeri at GE in 1978 and successfully completed the project in 1979. The results of the experiments were reported in 1979.

The device structure was referred to as a "V-groove MOSFET device with the drain region replaced by a p-type anode region" in this paper and subsequently as "the insulated-gate rectifier" (IGR), the insulated-gate transistor (IGT), the conductivity-modulated field-effect transistor (COMFET) and "bipolar-mode MOSFET".



The IGBT (insulated gate bipolar transistor) was developed in the late 1970s. Image courtesy of dpa picture aliance/Alamy

1989: FIN FIELD-EFFECT TRANSISTOR (FINFET)

A fin field-effect transistor (FinFET) is a multigate device, a MOSFET (metal-oxide-semiconductor field-effect transistor) built on a substrate where the gate is placed on two, three, or four sides of the channel or wrapped around the channel, forming a double or even multi-gate structure. These devices have been given the generic name "FinFETs" because the source/drain region forms fins on the silicon surface. Compared to CMOS devices, FinFET devices have significantly faster switching times and higher current density.

The first FinFET transistor type was called a "Depleted Lean-channel Transistor" or "DELTA" transistor, which was first fabricated in Japan by Hitachi Central Research Laboratory's Digh Hisamoto, Toru Kaga, Yoshifumi Kawamoto, and Eiji Takeda in 1989.

This article was originally published on DesignNews.com on December 9, 2022.

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Wednesday, February 1, 2023 | 10:00 am | Elizabeth A. Hangs Theater

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A Processing-In-Memory on High Bandwidth Memory (PIM-HBM): Impact of Interconnect Channels on System Performance in 2.5D/3D IC

Current Limitation and New Method to Accurately Estimate Reference Signal Jitter for 100+ Gbps 802.3 and OIF/CEI Interference Tolerance Test

Deep Reinforcement Learning-based Channel Flexible Equalization Scheme: An Application to High Bandwidth Memory

IBIS-AMI Modeling and Correlation Methodology for ADC-Based SerDes Beyond 100 Gb/s

Imitate Expert Policy and Learn Beyond: A Practical PDN Optimizer by Imitation Learning

Proper Ground Return Via Placement for 40+ Gbps Signaling

Thursday, February 1, 2023 | 10:00 am | Elizabeth A. Hangs Theater

The winner will be selected based on his or her leadership, creativity, and out-of-the-box thinking brought to design/test of chips, boards, or systems, with particular attention paid to areas of signal and power integrity.

Congratulations to these five exceptional finalists:
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Casey Morrison, Chief Product Officer and Co-Founder, Astera Labs
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Larry D. Smith, Principal Signal Integrity Engineer, Micron
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