DesignCon® 2022

WHERE THE CHIP MEETS THE BOARD

SANTA CLARA CONVENTION CENTER
SANTA CLARA, CA

CONFERENCE:
APRIL 5-7, 2022

EXPO:
APRIL 6-7, 2022

Register at DesignCon.com / #DesignCon

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COMMUNICATIONS SOLUTIONS

Curious about how we solve complex electronic design challenges?

Visit the newest technology demonstrations for connectors and cables at Booth #833

DesignCon® 2022

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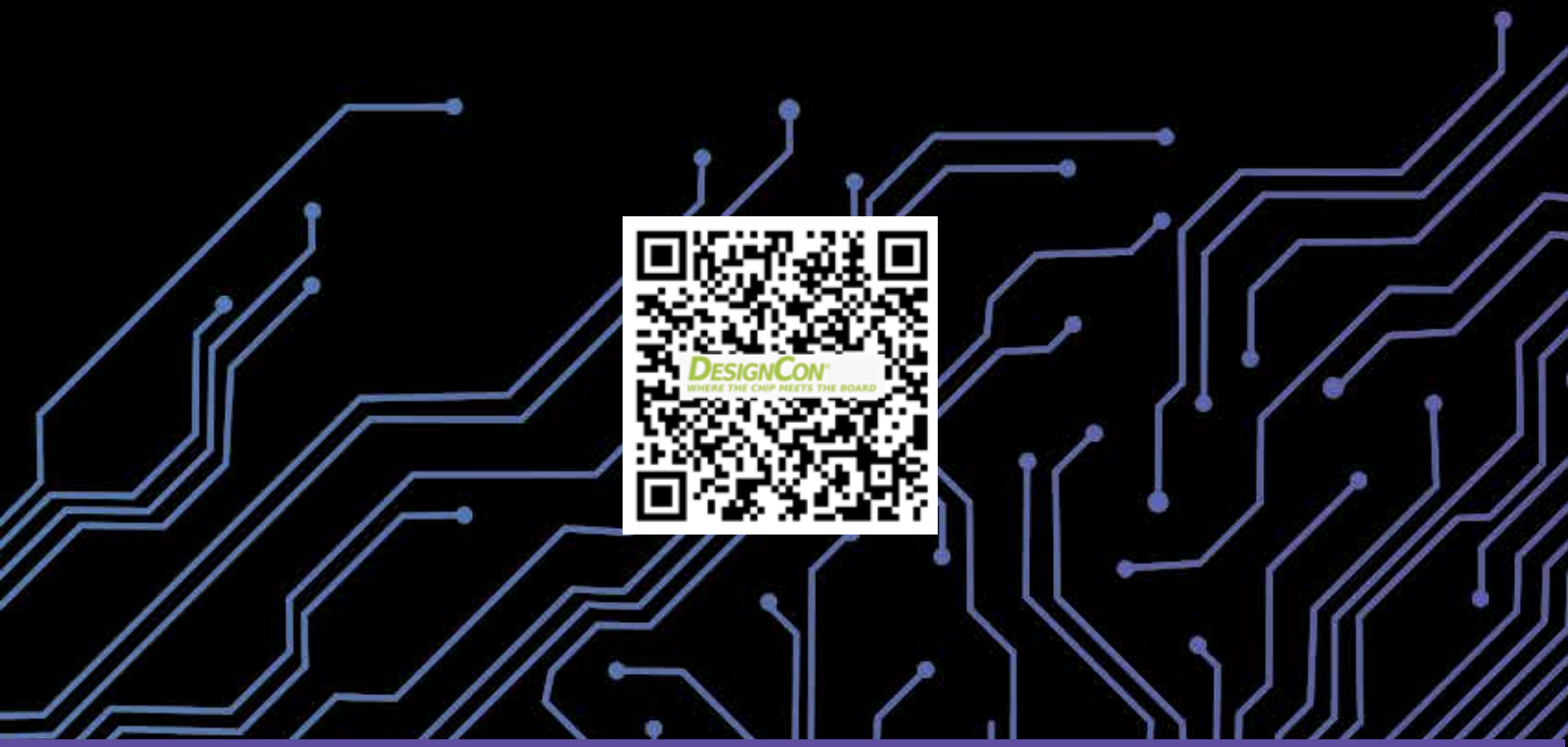
DesignCon 2022 is a Smart Event

Your access to DesignCon's education and expo doesn't end in Santa Clara!

After the in-person event, all attendees, speakers, and exhibitors will have access to our digital platform for recordings of select content from DesignCon, new education exclusively available online, networking opportunities, and exhibitor profiles, featuring white papers, product information, and more.

No need to register again – Your registration for the in-person event carries over to DesignCon's online offerings.

Scan the below for more information on DesignCon's online Smart Event offerings.



#DesignCon

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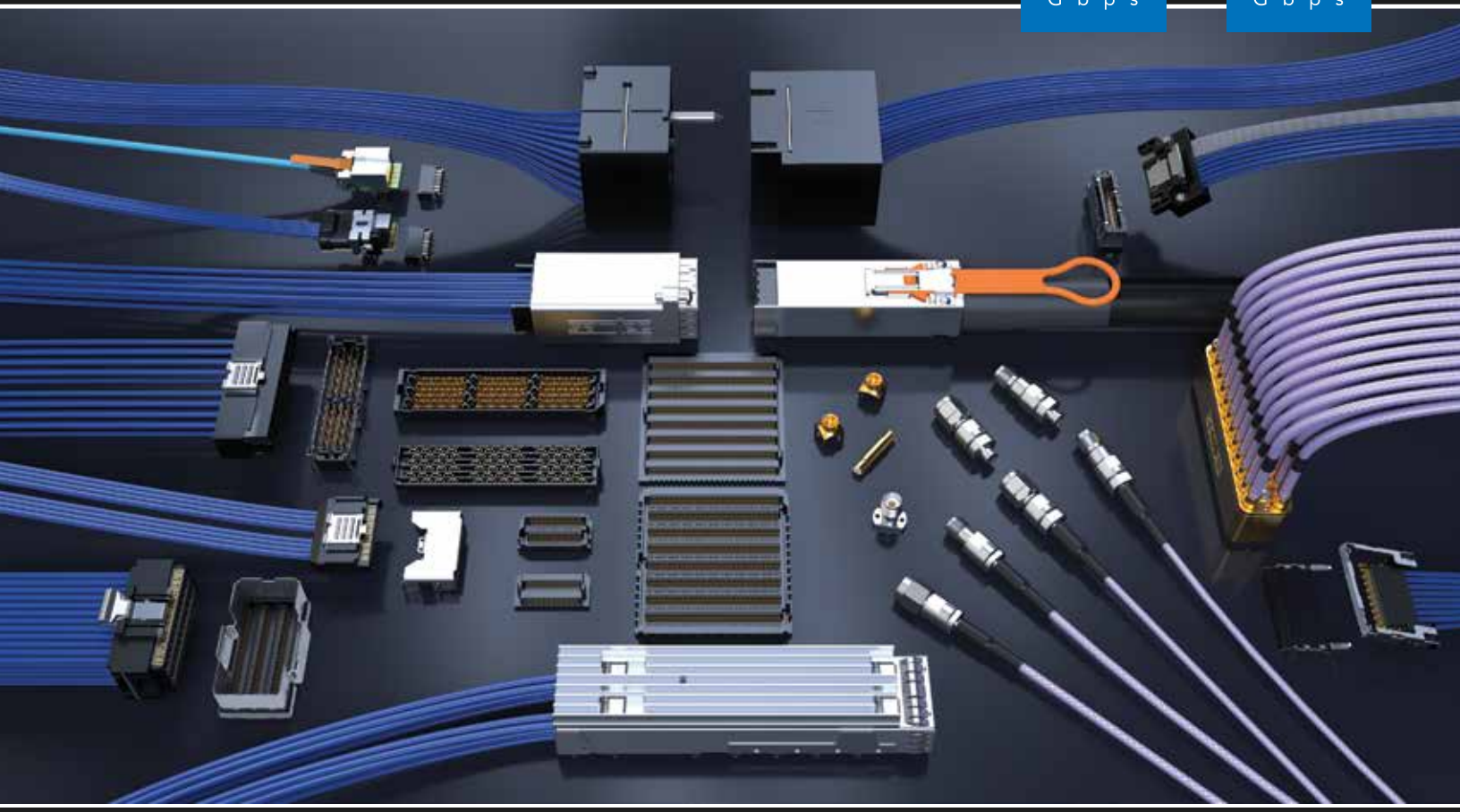
THE TECHNICAL RENAISSANCE IS SILICON-TO-SILICON SOLUTIONS

PAM4 112 Gbps → PAM4 224 Gbps



Samtec's Silicon-to-Silicon solutions exceed today's connectivity demands reaching 112 Gbps with a path of 224 Gbps and beyond.

samtec

BOOTH 939

Spring Break

WELCOME RECEPTION

TUESDAY, APRIL 5 | 6-8 PM

TERRA COURTYARD,
HYATT REGENCY SANTA CLARA

Sponsored By:

samtec

Enjoy complimentary cocktails, bites, games and more!

Open to all DesignCon, Drive World, and Embedded IoT World attendees, exhibitors, speakers, media, and committee members. (Badges required for entry.)

DesignCon® 2022
WHERE THE CHIP MEETS THE BOARD

#DesignCon

TPC MEMBERS

We would like to thank the volunteers who served on the Technical Program Committee (TPC) for DesignCon 2022. Their contributions as reviewers of the abstracts and papers have made it possible for us to maintain the DesignCon standard of excellence and deliver an outstanding program again this year.

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Joseph Aday*, Sr. Member of Technical Staff, Lockheed Martin
Maria Agoston*, Principal Engineer, Tektronix
Ravinder Ajmani, Technologist, Electronic Design Engineering, Western Digital
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Bruce Archambeault, Retired
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Ben Silva, Analog Engineer, Intel
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Chad Smutzer, Senior Engineer, Mayo Clinic
Mike Steinberger, Consulting Software Engineer, MathWorks
Ransom Stephens*, Consulting Senior Scientist at BitifEye Digital Solutions and Sage at Ransom's Notes
Changyi Su, Staff Design Engineer, AMD
Suresh Subramaniam, Principal Engineer/Architect, AMD
Madhavan Swaminathan, John Pippin Chair Professor in Microsystems Packaging & Emag, Georgia Tech
Donald Telian, Owner/Consultant, SiGuys
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Peter Tomaszewski, Sr Field Applications Engineer, Tektronix
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Iliya Zamek, Architect, Technical Manager, HCL America
Geoffrey Zhang, Distinguished Engineer and Supervisor, AMD
Pavel Zivny, Domain Expert, Tektronix

*2022 track co-chair

KEYSIGHT TECHNOLOGIES

Accelerate Your Fastest Digital Designs

EDUCATION FORUM

PCIe6

Power Integrity

Signal Integrity

Next-Gen Type-C

Next-Gen Memory

Forward Error Correction

April 7th

Visit Us in Mission City Ballroom B4

GENERAL INFORMATION

LOCATION & DATES
DesignCon will take place April 5-7, 2022, at the Santa Clara Convention Center in Santa Clara, CA. DesignCon welcomes Drive World and Embedded IoT World to this year's event.

CONFERENCE HOURS
Tuesday, April 5, 2022: 9:00 am – 6:00 pm
Wednesday, April 6, 2022: 8:00 am – 5:15 pm
Thursday, April 7, 2022: 8:00 am – 5:15 pm

EXHIBIT HOURS
Wednesday, April 6, 2022: 11:00 am – 6:00 pm
Thursday, April 7, 2022: 11:00 am – 6:00 pm

HEALTH & SAFETY
Health and safety are a top priority at this event. Visit DesignCon.com for up-to-date health and safety information and check the event app for any needed communications during the event.

REGISTRATION
Attendee, Speaker, Media and Exhibitor registration is located in Great America Ballroom J and X on the first floor of the convention center. Please present a photo ID when picking up your badge.

Tuesday, April 5: 7:00 am – 5:00 pm
Wednesday, April 6: 7:00 am – 6:00 pm
Thursday, April 7: 7:00 am – 6:00 pm

SMART EVENT
DesignCon is a smart event - a hybrid experience that extends the value of DesignCon beyond the three days in Santa Clara. As a pass holder you have access to our digital platform, Swapcard, where you can make connections with exhibitors, speakers and attendees; view product information; and watch exclusive content. Visit DesignCon.com for more details.

WELCOME RECEPTION
Enjoy complimentary cocktails, bites, games, and more at DesignCon's annual gathering on Tuesday, April 5, 6:00-8:00 pm on the Terra Courtyard at the Hyatt Regency. This year's open-to-all pass types reception is themed as a Spring Break for engineers. Badges required for entry.
Sponsored by: samtec

CONCESSIONS
Concessions are available in Exhibit Hall A in the Santa Clara Convention Center next to the Chiphead Theater.

CONFERENCE BREAKS
Conference breaks will be provided for paid conference passholders, event committee members and speakers. The breaks will be located in the conference hallways at the following times:

Tuesday, April 5:
Morning Break: 11:30 – 11:45 am
Afternoon Break: 4:30 – 4:45 pm

Wednesday, April 6 & Thursday, April 7:
Morning Breaks: 8:45 – 9:00 am, 9:45 – 10 am
Afternoon Breaks: 2:45 – 3:00 pm, 3:45 – 4:00 pm

CONFERENCE BREAKFAST
Complimentary breakfast is available on Tuesday, April 5 from 8:00 - 9:00 am in Mission City Ballroom B1 for all paid conference attendees, event committee members and speakers.

The program is subject to change without notice. Informa Markets reserves the right to alter venue, speakers, content, and/or other offerings.

Embedded IoT World

Taking place at DesignCon 2022 WHERE THE CHIP MEETS THE BOARD

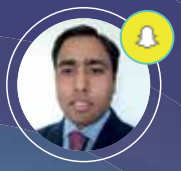
EMBEDDED SYSTEMS TO CREATE SAFE, RELIABLE & SECURE IOT

Take your embedded systems knowledge to the next level whilst at DesignCon at Embedded IoT World in Ballroom B, April 6 - 7. Curated by engineers, for engineers, learn directly from the technical specialists bringing end-to-end IoT to life and take back tangible ideas to propel your projects forward.

LEVEL-UP YOUR EXPERTISE AT SESSIONS LIKE:

WEDNESDAY APRIL 6, 2022

APP STARTUP COMPILER OPTIMIZATIONS & TECHNOLOGIES FOR EMBEDDED SYSTEMS

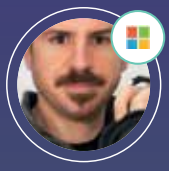


ADITYA KUMAR
Senior Software Engineer / Compiler Engineer
Snap Inc.

TOWARDS IOT DEVICE INTEGRATION IN SMART HOMES
(LUNCH INSIDER SESSION/WORKSHOP)

ALESSANDRO BASSANO
Principal Security Research Scientist
Technology Innovation Institute

LESSONS LEARNED FROM BUILDING A CONNECTED ARTIFICIAL NOSE USING TINYML



BENJAMIN CABE
Principal Program Manager, **Azure IoT Microsoft**

THURSDAY APRIL 7, 2022

SMOKE & MIRRORS: COMMUNICATION IN THE IOT WORLD

ROBERT HAFERNIK
Principal Key Expert Engineering
Siemens

IT'S JUST A VULNERABLE COMPUTER: PROTECTING AUTONOMOUS SYSTEMS

JULIA DOWNES
Principal Embedded Operating Systems Engineer
Defence Science & Technology Laboratory (GOV UK)

WANT TO PUT YOUR LEARNING INTO ACTION?

WHY NOT COME AND MEET OUR AWE-INSPIRING EXHIBITORS...

EMQ imec PARAGON INNOVATIONS SVT SVTRONICS, INC. TII Technology Innovation Institute

#EIOTWORLD

GENERAL INFORMATION

CONFERENCE NETWORKING LUNCH

Complimentary lunches are available daily for paid conference attendees, event committee members, and speakers.

Tuesday, April 5: Mission City Ballroom B1
Wednesday, April 6 & Thursday, April 7: Expo Floor

CHIPHEAD THEATER

Check out the specialty programming in the Chiphead Theater featuring panels, training, and more right on the expo floor.

Sponsored by: Amphenol

DRIVE WORLD

DesignCon welcomes Drive World back to the conference, offering an educational track for engineers looking to advance in the growing automotive electronics and intelligence industries. Drive World topics can be found under the session listings in this program. All DesignCon conference passholders have access to Drive World education.

Drive WORLD CONFERENCE

EMBEDDED IoT WORLD

Embedded IoT World, in partnership with DesignCon, provides a curated program for engineers, architects, and developers using embedded technologies to bring end-to-end IoT solutions to life. Free to explore for all pass holders, you'll be able to access technical sessions to build your expertise and learn how to tackle your biggest implementation challenges. You're also invited to discover new technologies and meet with key solution providers in silicon, chip design, semiconductors, processors, connectivity, and more on the expo floor.

Embedded IoT World

PRODUCT SHOWCASE

See live, interactive demos at exhibitor booths as companies give you a first-hand look at their latest products and features. Demo schedule can be found in the main agenda.

BOOTH BAR CRAWL

Wind down at daily meet-and-greets around the expo floor, from 5:00 – 6:00 pm, Wednesday and Thursday. Come for the conversation, stay for the bites and beverages. Please note that food will be provided around the expo floor.

Sponsored by: Amphenol CARLISLE INTERCONNECT TECHNOLOGIES Tektronix ACE ACCURATE CIRCUIT ENGINEERING Rosenberger Ansys

PRESENTATION DOWNLOAD

Use the QR code below to download select speaker presentations. Note: Some presentations are available only for paid conference attendees. Login information will be emailed to paid conference attendees ahead of the event.

DesignNews

2022

CEC Continuing Education Center

The Digi-Key Continuing Education Center, presented by Design News, is a well-established, highly technical program with an extensive archive of content at your disposal.

Our highest-attended courses include: Raspberry PI, IoT Device Prototyping, Embedded Software Development Design Techniques, and many more.

5-DAY COURSES

- Earn Free IEEE credits
- Access to entire course archive
- Interactive chat session to tackle and solve technical issues
- Download additional learning materials

REGISTER TODAY

www.designnews.com/continuing-education-center

SPEAKERS:

FRED EADY

Principal Engineer

Georgia Branch of Ongoing Systems

JACOB BENINGO

Embedded Software Consultant

Beningo Embedded Group

DON WILCHER

Electrical Engineer, Technical Author & Researcher

MaDon Research

GENERAL INFORMATION

APP
This event utilizes a smartphone app to convey any event changes, as well as provide information, such as session details, expo maps, and hours.

Search “Informa Markets Events” in the app store to download, then log-in using the same email address you used to register for this event and select “DesignCon” from the event choices.

EVALUATIONS
We value attendee feedback when planning the conference. Conference attendees can evaluate sessions using the below QR code.

INFORMATION DESK
There is an information desk available in the Conference Hallway near the entrance to the Mission City Ballroom and another on the expo floor in the Design News Lounge. Stop by if you have any questions on the event or need to speak to a member of event management.

INTERNET ACCESS
Wireless internet access is available throughout the building. Please use username “DesignCon” and password “amphenol” for access.

LOST & FOUND
Lost and found is located at Registration.

PUBLIC TRANSPORTATION & PARKING
Information on public transportation and the event’s parking rates can be found on DesignCon.com’s Plan Travel tab.

MINORS
For safety, insurance, and security reasons, no one under the age of 18 is permitted in the expo halls or conference meeting rooms at the event. No childcare services are available onsite.

MEDIA CENTER
Located in Mission City Ballroom M1 and M2, the Media Center is open to registered exhibitors and their representatives, as well as members of the press and analysts. You must have a media badge for access. If you would like to set up any meetings please reach out to: pr.ime@informa.com.

SPEAKER CENTER
Located in Mission City Ballroom M1 and M2, the Speaker Center is open to registered speakers, as well as members of the DesignCon committees. You must have a speaker badge or be a current committee member for access.

DON'T MISS

INSTANT INSIGHTS MEETS IN-DEPTH INFORMATION

Attend the full-day seminar series
Wednesday, April 6th | 8am-5pm
Great America Meeting Room 2

VISIT BOOTH #1049

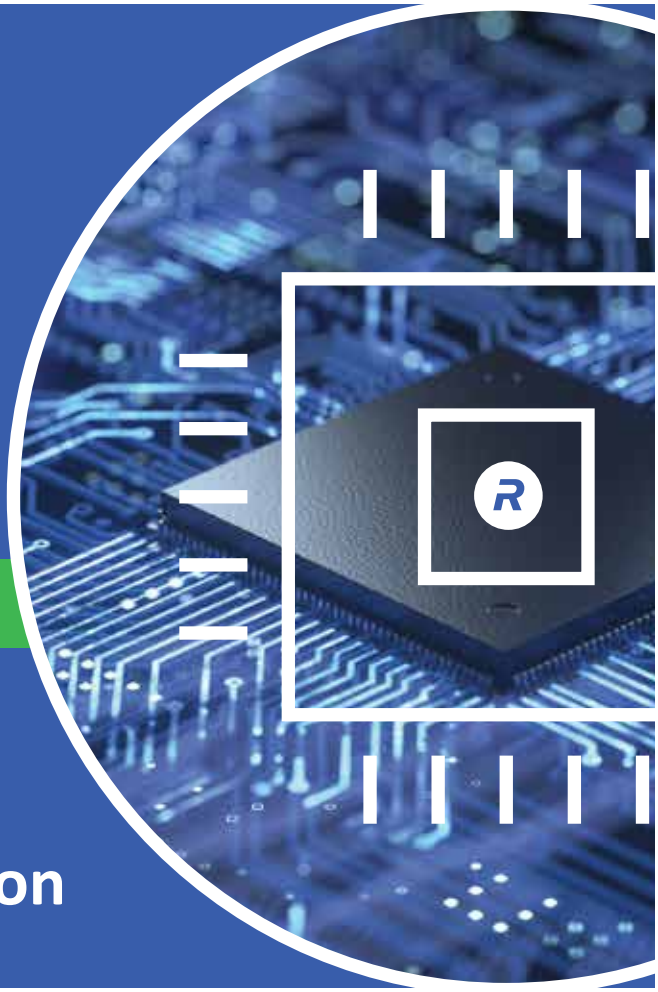
INTRODUCING THE R&S®RTO6 OSCILLOSCOPE SERIES

ROHDE&SCHWARZ

Rambus

SerDes & Memory Interfaces

A comprehensive suite of SerDes and memory interface IP for today's most challenging data center, edge, automotive and IoT applications.



RAMBUS TECHNICAL SESSIONS

Wednesday, April 6
Room: Great America 1

rambus.com/designcon

DesignCon® 2022

WHERE THE CHIP MEETS THE BOARD

KEYNOTES Open to All Attendees

John Bowers
Fred Kavli Chair of Nanotechnology
University of California
Santa Barbara

Progress Enabled: The Convergence of Photonic & Electronic ICs

Tuesday, April 5, 2022
12:00 pm-12:45 pm
Elizabeth A. Hangs Theater

Advancements are happening that will drive the future direction of the data center, and put silicon photonics at the heart of this push. The current convergence of progress in silicon photonics and electronics means that co-packaged silicon photonics and electronics enable the continued progress of both fields and propel further innovation in both.

Laurence Moroney
Artificial Intelligence Lead
Google

The Realities of AI & Machine Learning: Cut Through the Hype & Move to Production

Wednesday, April 6, 2022
10:00-11:00 am
Elizabeth A. Hangs Theater

We've all heard about the potential of AI and machine learning. Learn from a developer's perspective how machine learning can give a new programming paradigm that makes AI possible and enables problem solving that was previously infeasible.

This keynote is preceded by the Best Paper Award presentation.

José Morey
Consultant for NASA, IBM, Hyperloop Transportation, Liberty BioSecurity Health and Technology

Space Tech: Present & Future

Thursday, April 7, 2022
10:00-11:00 am
Elizabeth A. Hangs Theater

The rapid commercialization of space has gone beyond creating the first quadrillion dollar industry and developed the first truly limitless economy. In this talk we will explore the technology and innovations that are bringing about a truly consequential change for our civilization.

This keynote is preceded by the Engineer of the Year Award presentation.

DESIGNCON® 2022
WHERE THE CHIP MEETS THE BOARD

April 5-7, 2022
Santa Clara Convention Center
Santa Clara, CA

JOIN US!

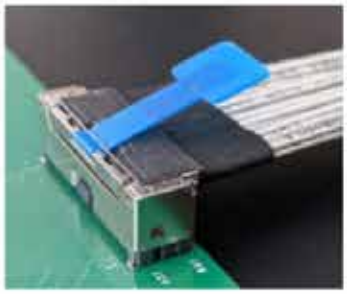
Luxshare-Tech at Booth #839

DesignCon.com/SPECIAL ▶ **REGISTER NOW**

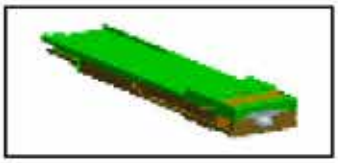
Luxshare-Tech proudly presents our latest technology in interconnects and cable assemblies at DesignCon 2022. Our recent product release includes up to 112G PAM4 DACs and Active Copper Cables (ACC) using Luxshare' s own OptamaxTM bulk cable and QSFP112G DR4 modules. Please stop by our booth at DesignCon (booth #839) to experience our exciting live demos.

LUXSHARE-Tech' s 112G PAM4 direct attached passive copper cable assemblies enable next generation high-speed data communication. By combining eight channels, operating at speeds up to 112 Gbps per lane into one affordable high-density media data interface (MDI) and providing aggregate data throughput in excess of 800 Gbps. Leveraging LUXSHARE' s own proprietary OptamaxTM ultra low loss twin-axial raw cable, and carefully designed MSA compliant paddle card and cage technology, LUXSHARE-Tech' s 112G PAM4 DACs over industry leading signal integrity and thermal performance for server, storage, and switch applications.

For more information



Our internal high speed interconnect solution supports next generation servers using our OmniEdgeTM family of products. In addition we offer MCIO, GEN-Z cable, and SlimSAS cable assemblies and board connectors supports up to PCIE 6.0; Low profile SlimSAS cable assemblies and board connectors supports up to SAS4.0, with anti-skew interface.



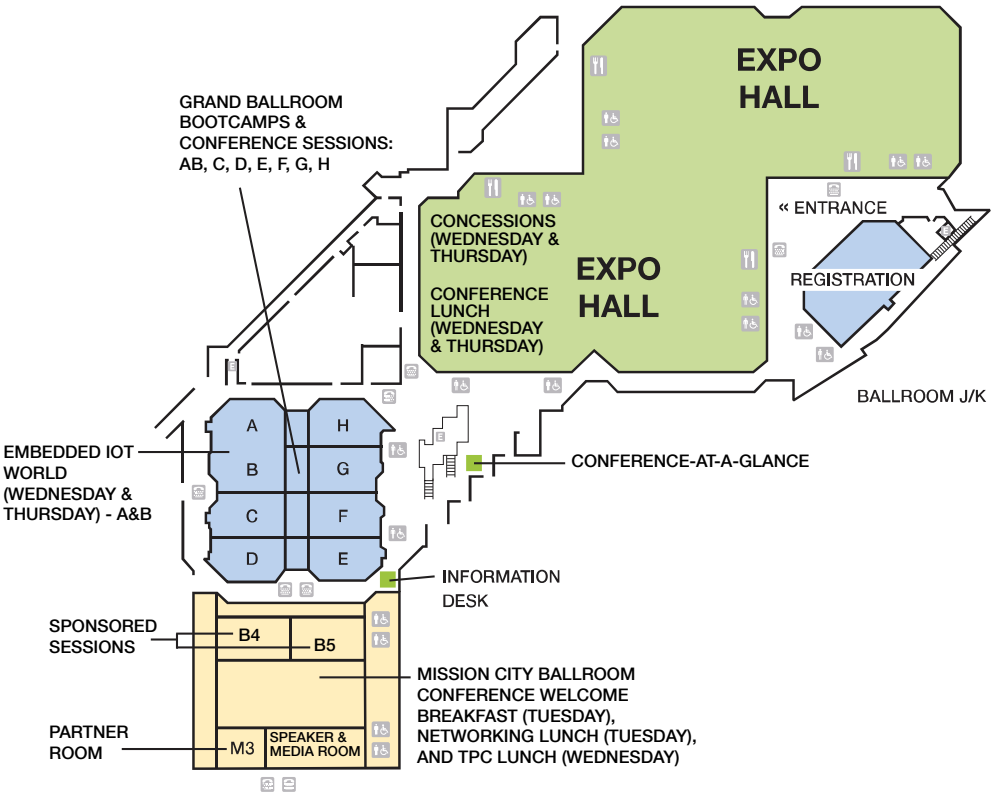
Luxshare' s copper loopbacks are offered in QSFP-DD / QSFP28/ SFP28 form factors. Our loopbacks support adjustable power consumption optimizing switch verification to be more cost-effective.

Luxshare-Tech' s optics supports 10G to 400G data rate, for the applications over 1,000 meters connectivity length.

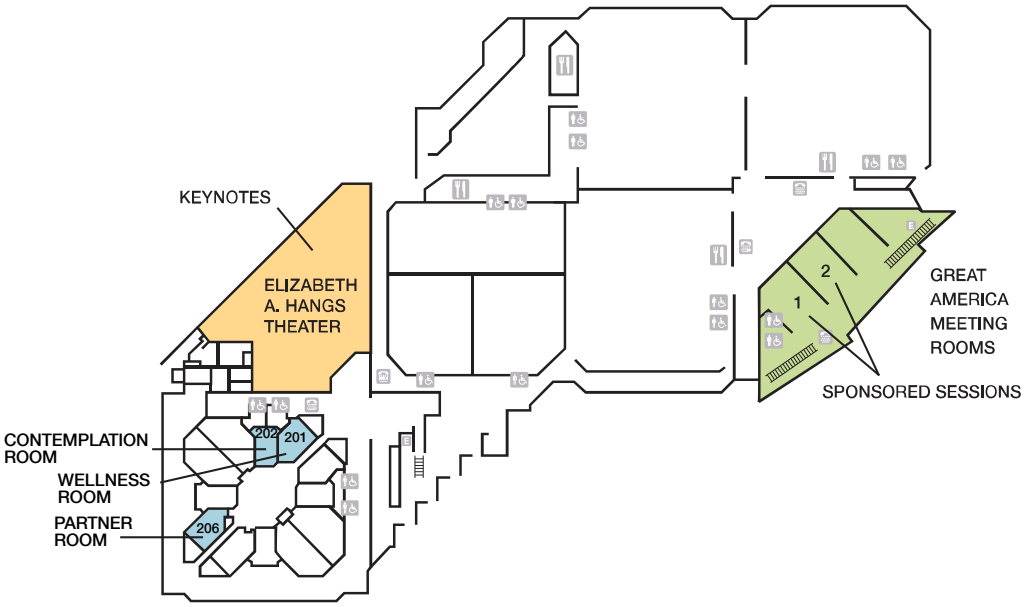
480 N. McCarthy Blvd #280, Milpitas, CA http://www.luxshare-tech.com/

CONFERENCE MAP

FIRST FLOOR



SECOND FLOOR



SESSIONS – TUESDAY, APRIL 5

8:00 AM – 9:00 AM

Networking Session
Conference Welcome Breakfast
All Access Pass — Mission City Ballroom B1

9:00 AM – 4:30 PM

14 Boot Camp – AI & Deep Learning for SI/PI
1 All Access Pass — Ballroom GH

9:00 AM – 11:30 AM

8 Tutorial – Design & Verification for High-Speed I/Os at 10 to 112 & 224Gbps with Jitter, Signal Integrity & Power Optimized
All Access Pass — Ballroom EF

9 Tutorial – PAM6 Signaling: A Potential Candidate at 224Gbps
7 All Access Pass — Ballroom AB

12:00 PM – 12:45 PM

★ Keynote – Progress Enabled: The Convergence of Photonic & Electronic ICs
3 Open to All — Elizabeth A. Hangs Theater

12:30 PM – 2:30 PM

Networking Session
Conference Networking Lunch
All Access Pass — Mission City Ballroom B1

2:00 PM – 4:30 PM

13 Tutorial – OSFP/QSFP-DD 112G PAM4 Channel for 800G System Applications
7 All Access Pass — Ballroom AB

3 Tutorial – Over the Air Testing of 5G AiP Modules in High-volume Manufacturing
All Access Pass — Ballroom D

10 Tutorial – The Real World of Power Integrity & Signal Integrity Working Together
All Access Pass — Ballroom EF

4:45 PM – 6:00 PM

2 Panel – AMI Models & the Seven-year Itch
7 Open to All — Ballroom AB

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

- D Drive World — Advanced Automotive
- E Embedded IoT World
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- General Event
- ★ Special Event
- Sponsored Sessions

SESSIONS – TUESDAY, APRIL 5

4:45 PM – 6:00 PM

Panel – CXL & PCIe Technologies: The Next Generation of Interconnects
5 7
Open to All — Ballroom EF

Panel – The Case of the Closing Eyes: PAM-N, What Can be Tested?
8 12
Open to All — Ballroom GH

Panel — Bringing AI to the Edge: Hardware & Software Enables Autonomous AI Ecosystem on the Edge
D
Open to All — Ballroom C

6:00 PM – 8:00 PM

Networking Session
Welcome Reception
Open to All — Terra Courtyard at the Hyatt Regency

Sponsored by: samtec

TRACKS AND LEGEND

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1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
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11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
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- D Drive World — Advanced Automotive
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- Best Paper Awards Finalist
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- Chiphead Theater Presentation
- General Event
- Special Event
- Sponsored Sessions

SESSIONS – WEDNESDAY, APRIL 6

8:00 AM – 8:45 AM

A New Challenge for Neuromorphic Computing Systems: From Off-chip Interconnects to On-chip Interconnects
All Access Pass, 2-Day Pass — Ballroom D

A Processing-In-memory on High-bandwidth Memory (PIM-HBM): Impact of Interconnect Channels on System Performance in 2.5D/3D IC
All Access Pass, 2-Day Pass — Ballroom G

A Step-by-step Guide to a Novel Lab Correlated PDN Co-simulation Methodology
All Access Pass, 2-Day Pass — Ballroom F

Onchip ESD Protection Structure Modeling Methodology
All Access Pass, 2-Day Pass — Ballroom E

Validation of Achieving 200Gbps Signaling per Electrical Lane Over 1 Meter of Passive Twinaxial Copper Cable
All Access Pass, 2-Day Pass — Ballroom H

Challenges & Solutions in Physical Layer Testing for Automotive Wired Communications
All Access Pass, 2-Day Pass — Ballroom C

8:00 AM – 8:40 AM

In-Situ De-embedding
Open to All — Great America Meeting Room 2

9:00 AM – 9:45 AM

Accurate Correlation Between SI Simulation & Measurement in High-speed Backplane Connector Designs
All Access Pass, 2-Day Pass — Ballroom G

DDR4-3200 FPGA-based System with Interposer Power Aware SI Simulation to Measurement Correlation
All Access Pass, 2-Day Pass — Ballroom E

Generalized ccICN (Component Contribution Integrated Crosstalk Noise)
All Access Pass, 2-Day Pass — Ballroom H

Integration-based Method for Surface Roughness Modeling of Copper Foils
All Access Pass, 2-Day Pass — Ballroom D

Optimal Design of High-Speed Flexible Interconnectors by Applying Bayesian Optimization & 3D Electromagnetic Solvers
All Access Pass, 2-Day Pass — Ballroom F

Multi-Sensor Safety Calibration for ADAS Applications
All Access Pass, 2-Day Pass — Ballroom C

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

- D Drive World — Advanced Automotive
- E Embedded IoT World
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- General Event
- Special Event
- Sponsored Sessions

SESSIONS – WEDNESDAY, APRIL 6

9:00 AM – 9:40 AM

Developing High-Quality Test Fixtures for De-embedding of S-Parameters
Open to All — Great America Meeting Room 2

10:00 AM – 11:00 AM

Keynote – The Realities of AI & Machine Learning: Cut Through the Hype & Move to Production
Open to All — Elizabeth A. Hangs Theater

11:00 AM – 6:00 PM

Expo Hall Open
Open to All — Expo Floor

11:00 AM – 11:10 AM

Chairperson's Opening
Open to All — Ballroom B

11:10 AM – 11:40 AM

Towards Open-source Edge-cloud Collaboration Architecture
Open to All — Ballroom B

11:10 AM – 11:50 AM

Test compliance automation solution for high-speed Ethernet interconnects using ZNrun
Open to All — Great America Meeting Room 2

11:15 AM – 12:00 PM

Improved Methodology to Accurately Perform System Level Power Integrity Analysis Including an ASIC Die
All Access Pass, 2-Day Pass — Ballroom F

Learning Super-scale Microbump Pin Assignment Optimization for Real-world PCB Design with Graph Representation
All Access Pass, 2-Day Pass — Ballroom E

Long-haul Inter-domain Power Noise
All Access Pass, 2-Day Pass — Ballroom H

Performance Assessment of W-band Antennas on Low-loss Inhomogeneous PCB Substrates
All Access Pass, 2-Day Pass — Ballroom D

Receiver Calibration & Testing Methodologies Comparison for PAM-4 IOs
All Access Pass, 2-Day Pass — Ballroom G

Making Transit Modernization Accessible: Lessons Learned
All Access Pass, 2-Day Pass — Ballroom C

Improving AR/VR Reality with 3D Time of Flight Sensing
Open to All — Chiphead Theater

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SESSIONS – WEDNESDAY, APRIL 6

11:40 AM – 12:10 PM

App Startup Compiler Optimizations & Techniques for Embedded Systems
Open to All — Ballroom B

12:10 PM – 12:40 PM

The Great Chip Storage - ways to manage supply issues in IoT.
Open to All — Ballroom B

12:10 PM – 12:50 PM

Power integrity measurement fundamentals
Open to All — Great America Meeting Room 2

12:15 PM – 1:00 PM

A Comprehensive Study About Inhomogeneous Dielectric Layers (IDLs) & the Impacts on Far-end Crosstalk of High-speed PCB Striplines
All Access Pass, 2-Day Pass — Ballroom G

Challenges of Automated Stressed Receiver Tolerance Testing: NRZ, PAM4 & Beyond
All Access Pass, 2-Day Pass — Ballroom F

How A Standards-Based Framework Can Simplify Camera & Display Integration in Automotive Architectures
All Access Pass, 2-Day Pass — Ballroom C

In Search of the Holy Grail: Laminate Dk & Df Values that You Can Trust
Open to All — Chiphead Theater

12:15 PM – 1:00 PM

Next Generation 224Gbps-PAM4 SERDES, Channel & Link Systems
All Access Pass, 2-Day Pass — Ballroom H

Noise Coupling Path Visualization for Complex Electronic Systems
All Access Pass, 2-Day Pass — Ballroom E

Parametric System Model of a 112Gbps ADC-based SerDes for Architectural, Design & Validation Project Phases
All Access Pass, 2-Day Pass — Ballroom D

12:30 PM – 2:30 PM

Networking Session
Conference Networking Lunch
All Access Pass, 2-Day Pass — Expo Floor

12:40 PM – 1:20 PM

Panel – Processing Data at the Edge with Your Embedded Device
Open to All — Ballroom B

1:15 PM – 2:00 PM

Limits of High-speed Connector & Cable Technology
Open to All — Chiphead Theater

TRACKS AND LEGEND

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SESSIONS – WEDNESDAY, APRIL 6

1:20 PM – 2:35 PM

(E) Sponsored Lunch Workshop Session: Towards IoT Devices Integration in Smart Homes
Open to All — Ballroom B

2:00 PM – 2:40 PM

(🔗) A comparison of solutions for jitter and noise separation
Open to All — Great America Meeting Room 2

2:00 PM – 2:45 PM

(11) (12) EMI Qualification of QSFP & OSFP Electrical/optical Modules
All Access Pass, 2-Day Pass — Ballroom E

(🎖) (3) (6) Impacts of Interferences & Crosstalk from Adjacent Optical Channels on High-Performance Silicon Photonic Transceiver
All Access Pass, 2-Day Pass — Ballroom G

(4) (13) PCB Manufacturing Design Guidelines for Cost Reduction in Immersion Cooling
All Access Pass, 2-Day Pass — Ballroom D

(14) (10) Security Integrity Analytics by Thermal Side-channel Simulation: An ML-augmented Auto-POI Approach
All Access Pass, 2-Day Pass — Ballroom H

(🎖) (12) VNA Calibration Essentials for Practicing Engineers
All Access Pass, 2-Day Pass — Ballroom F

2:00 PM – 2:45 PM

(D) PCI Express Technology: Evolving Automotive Connectivity for the Next Generation of Vehicles
All Access Pass, 2-Day Pass — Ballroom C

2:15 PM – 3:00 PM

(🎭) New System-level Opportunities with OSFP-XD
Open to All — Chiphead Theater

2:35 PM – 3:05 PM

(E) Lessons learned from building a connected artificial nose using TinyML
Open to All — Ballroom B

(🔗) Automotive High-Speed Signal Protocols & Standards
Open to All — Mission City Ballroom B4

3:00 PM – 3:45 PM

(1) (10) A Comparison of Motherboard Voltage Regulators & Fully Integrated Voltage Regulators for Power & Performance Optimized Solutions
All Access Pass, 2-Day Pass — Ballroom D

(10) (6) PDN Design Optimization from an IC to a PCB for a Mixed-reality Display Subsystem
All Access Pass, 2-Day Pass — Ballroom E

(🎖) (7) (13) Proper Ground Return Via Placement for 40+ Gbps Signaling
All Access Pass, 2-Day Pass — Ballroom F

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App

(1) Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
(2) Chip I/O & Power Modeling
(3) Integrating Photonics & Wireless in Electrical Design
(4) Advances in Materials & Processing for PCBs, Modules & Packages
(5) Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
(6) System Co-Design: Modeling, Simulation & Measurement Validation
(7) Optimizing High-Speed Link Design
(8) Measurement & Simulation Techniques for Analyzing Jitter, Noise & BER
(9) High-Speed Signal Processing, Equalization & Coding/FEC
(10) Power Integrity in Power Distribution Networks
(11) Electromagnetic Compatibility & Interference
(12) Applying Test & Measurement Methodology
(13) Modeling & Analysis of Interconnects
(14) Machine Learning for Microelectronics, Signaling & System Design

(D) Drive World — Advanced Automotive
(E) Embedded IoT World
(🎖) Best Paper Awards Finalist
(🥾) Boot Camp
(🎭) Chiphead Theater Presentation
(📅) General Event
(★) Special Event
(🔗) Sponsored Sessions

SESSIONS – WEDNESDAY, APRIL 6

3:00 PM – 3:45 PM

Three Very Low-cost Technology Solutions for SI Applications
All Access Pass, 2-Day Pass — Ballroom H

Validation Shift-left: Enabling Early SerDes Mixed-signal Validation
All Access Pass, 2-Day Pass — Ballroom G

Building Safe & Secure Systems Using Open Source
All Access Pass, 2-Day Pass — Ballroom C

3:00 PM – 3:40 PM

Practical signal integrity measurements on embedded serial interfaces
Open to All — Great America Meeting Room 2

3:05 PM – 3:35 PM

Augmented-Reality Optical Narrowcasting (ARON)
Open to All — Ballroom B

3:15 PM – 4:00 PM

Bespoke Silicon: How Systems Companies are Driving Chip Design
Open to All — Chiphead Theater

3:35 PM – 4:05 PM

How to Select the Best RTOS for your Connected Device
Open to All — Ballroom B

4:00 PM – 4:40 PM

Automotive Ethernet MGBase-T Compliance testing
Open to All — Great America Meeting Room 2

4:00 PM – 5:15 PM

Panel – AI & Digital Twins for SI/PI Analysis & Design
Open to All — Ballroom G

Panel – Modeling Passive Component for Power Integrity Simulations: How to Measure, How to Model, How to Use
Open to All — Ballroom H

Panel – OIF Electrical I/O Specifications: Progress on CEI 112Gbps & 224Gbps
Open to All — Ballroom D

Panel – Implementing a Digital Transformation Framework for Automotive Applications
Open to All — Ballroom C

TRACKS AND LEGEND

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1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
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- E Embedded IoT World
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SESSIONS – WEDNESDAY, APRIL 6

4:15 PM – 5:00 PM

Production ML for Mission-Critical Applications
Open to All — Chiphead Theater

5:00 PM – 6:00 PM

Networking Session
Booth Bar Crawl
Open to All — Expo Floor

Sponsored by: Amphenol, CARLISLE INTERCONNECT TECHNOLOGIES, Tektronix®, ACE ACCURATE CIRCUIT ENGINEERING

TRACKS AND LEGEND

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SESSIONS – THURSDAY, APRIL 7

8:00 AM – 8:45 AM

112G-PAM4-QSFP Interconnect: A Study in Air Cooling & Immersion Cooling
All Access Pass, 2-Day Pass — Ballroom F

Equalizer (Tx/Rx) Optimization at 112Gbps
All Access Pass, 2-Day Pass — Ballroom H

Imitate Expert Policy & Learn Beyond: A Practical PDN Optimizer by Imitation Learning
All Access Pass, 2-Day Pass — Ballroom D

Imitation Learning with Bayesian Exploration (IL-BE) for Signal Integrity (SI) of PAM-4 based High-speed Serial Link: PCIe 6.0
All Access Pass, 2-Day Pass — Ballroom G

PCB Stackup & Launch Optimization in High-speed PCB Designs
All Access Pass, 2-Day Pass — Ballroom E

Open Standard Acceleration APIs for Safety-Critical Graphics, Vision & Compute
All Access Pass, 2-Day Pass — Ballroom C

9:00 AM – 9:45 AM

How to Optimize TxFFE & What We Can Learn From the Optimization
All Access Pass, 2-Day Pass — Ballroom E

Magnetic Near-field Evaluation Methodology for Integrated Circuit In-package Coupling Assessment
All Access Pass, 2-Day Pass — Ballroom D

New Power Integrity Methodology & Mitigation Effect of PDN Voltage Decay
All Access Pass, 2-Day Pass — Ballroom G

Understanding S Parameters in Time Domain & the Application to Two X Automatic Fixture Removal of High-speed Interconnects
All Access Pass, 2-Day Pass — Ballroom F

Understanding the Effect of Temperature on Permittivity & Loss of Dielectric Substrates
All Access Pass, 2-Day Pass — Ballroom H

Enhancing Safety & Performance in ADAS/AV with a Motion First Approach to Perception
All Access Pass, 2-Day Pass — Ballroom C

No Exit Ramps Needed-Cadence's System Design Workflow Delivers Seamless In-Design Analysis, Reducing Turnaround Time and Minimizing Risk
Open to All — Mission City Ballroom B5

TRACKS AND LEGEND

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SESSIONS – THURSDAY, APRIL 7

10:00 AM – 11:00 AM

★ **Keynote – Space Tech: Present & Future**
Open to All — Elizabeth A. Hangs Theater

11:00 AM – 6:00 PM

Expo Hall Open
Open to All — Expo Floor

11:00 AM – 11:25 AM

E **Chairperson's Opening - Semiconductor Update**
Open to All — Ballroom B

11:00 AM – 11:45 AM

Overview and Challenges of Running D2D over Interposers
Open to All — Mission City Ballroom B5

11:15 AM – 12:00 PM

2 **COM-based IBIS-AMI for 106/112Gbps System Compliance**
All Access Pass, 2-Day Pass — Ballroom D

14 **Data-Efficient Machine Learning Method for Hardware Routing: Signal Integrity Demonstration to 2PDC and PCIe 6.0**
All Access Pass, 2-Day Pass — Ballroom E

10 2 **Practical Methods of Estimating Dynamic Current for Calculating PDN Target Z**
All Access Pass, 2-Day Pass — Ballroom H

11:15 AM – 12:00 PM

1 **Thermal Transmission Line: Smoothing Thermal Gradients & Lowering Temperature for Signal Integrity Improvement of HBM & 2.5D ICs**
All Access Pass, 2-Day Pass — Ballroom F

8 12 **Transmitter Jitter Measurement Methodologies for PAM-4 IOs**
All Access Pass, 2-Day Pass — Ballroom G

D **Moving Towards High Resolution Automotive Radar Systems**
All Access Pass, 2-Day Pass — Ballroom C

Five Tips for Power Integrity Measurements on a Budget
Open to All — Chiphead Theater

11:25 AM – 11:55 AM

E **Smoke and Mirrors: communication in the IoT world**
Open to All — Ballroom B

11:55 AM – 12:25 PM

E **It's just a Vulnerable Computer: Protecting Autonomous Systems**
Open to All — Ballroom B

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SESSIONS – THURSDAY, APRIL 7

12:00 PM – 2:45 PM

Addressing 112G Connector+PCB Modeling Without Having to Simulate with Terabyte Servers
Open to All — Mission City Ballroom B5

12:15 PM – 12:25 PM

A Study on 224G Channel Characteristics
6 Open to All — Chiphead Theater

12:15 PM – 1:00 PM

Automotive Semis Shifts into Overdrive
All Access Pass, 2-Day Pass — Ballroom C

Electro-optic & Custom Photonic Co-design in Monolithic Silicon Photonics Technology
3 6 All Access Pass, 2-Day Pass — Ballroom E

Investigation of Low-etch or Non-oxide Surface Treatment on Stripline Insertion Loss
4 7 All Access Pass, 2-Day Pass — Ballroom G

Reflecting on Reflections: An Evaluation of New & Standardized Metrics
7 8 All Access Pass, 2-Day Pass — Ballroom D

System Co-design for Sleek Detachable/tablet Reference Design
6 All Access Pass, 2-Day Pass — Ballroom F

12:15 PM – 1:00 PM

Transient vs. Statistical: A Comparative Study on Practical Parallel Link Qualification Techniques
8 13 All Access Pass, 2-Day Pass — Ballroom H

12:25 PM – 12:35 PM

De-embedding Method for 224G High Bandwidth
12 Open to All — Chiphead Theater

12:25 PM – 12:55 PM

Symmetrical Multi-Processing (SMP) with FreeRTOS and Raspberry Pi Pico
Open to All — Ballroom B

12:30 PM – 2:30 PM

Networking Session
Conference Networking Lunch
All Access Pass, 2-Day Pass — Expo Floor

12:35 PM – 12:45 PM

Optimal PDN Design Method for Mobile Phone Based on Q-learning Algorithm with Dynamic PI Simulation
10 Open to All — Chiphead Theater

12:55 PM – 1:35 PM

Equipment Teardown Session by Omdia
Open to All — Ballroom B

TRACKS AND LEGEND

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SESSIONS – THURSDAY, APRIL 7

1:00 PM – 1:45 PM

MIPI C-PHY System Design Exploration and Optimization for Signal Integrity Analysis by Using Advanced Cadence Compliance Kit
Open to All — Mission City Ballroom B5

1:15 PM – 2:00 PM

400/800GbE Interconnects: The Challenges & Resolutions for Cabling Complexity, Serviceability & Rack Power
Open to All — Chiphead Theater

2:00 PM – 2:45 PM

224Gbps-PAM4 End-to-end Channel Solutions for High-density Networking System
All Access Pass, 2-Day Pass — Ballroom H

Applications of High Bandwidth AWGs in Receiver Testing: Tricks of the Trade
All Access Pass, 2-Day Pass — Ballroom E

Current Limitation & New Method to Accurately Estimate Reference Signal Jitter for 100+ Gbps 802.3 & OIF/CEI Interference Tolerance Test
All Access Pass, 2-Day Pass — Ballroom D

2:00 PM – 2:45 PM

Effective Intra-pair Skew, EIPS & Intra-pair Skew Modeling Method
All Access Pass, 2-Day Pass — Ballroom G

Novel Power-integrity Solutions for Multi-HSIO with Silicon Co-relation
All Access Pass, 2-Day Pass — Ballroom F

Measurements & Test of High Speed Serial Buses: Measurement Bandwidth in Ethernet for Automotive, Electrical & Optical
All Access Pass, 2-Day Pass — Ballroom C

Mainstream Signal Integrity Workflow for PCIe 6.0 PAM4 Signaling
Open to All — Mission City Ballroom B5

2:15 PM – 3:00 PM

The Next Tipping Point for Semiconductors
Open to All — Chiphead Theater

2:35 PM – 3:05 PM

Providing the Best Industrial IoT Gateway Platforms for Device Connectivity & Management
Open to All — Ballroom B

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SESSIONS – THURSDAY, APRIL 7

3:00 PM – 3:45 PM

A T-coil Enhanced 18Gbps Memory Interface with Tx Bandwidth Extension & Rx Training Technique
All Access Pass, 2-Day Pass — Ballroom E

Experiment & Simulation Studies on Resonances due to Period Structure in PCBs
All Access Pass, 2-Day Pass — Ballroom D

Exploring the Requirements for 224Gbps Channel Characterization Using Simulations & Measurements
All Access Pass, 2-Day Pass — Ballroom F

IBIS-AMI Modeling & Correlation Methodology for ADC-Based SerDes Beyond 100Gbps
All Access Pass, 2-Day Pass — Ballroom G

Optimization of a Co-packaged Laser Module Design Using Statistical Analysis for Signal Integrity
All Access Pass, 2-Day Pass — Ballroom H

Role of Open Standards for the Long-term Sustainability of Networking Technologies
All Access Pass, 2-Day Pass — Ballroom C

The Future of 224G Serial Links
Open to All — Mission City Ballroom B5

3:05 PM - 3:35 PM

Securing the compute edge: A proactive process that takes forethought, planning, preparation, and execution
Open to All — Ballroom B

3:15 PM – 4:00 PM

Panel – AI/Robotics Startups That Support Manufacturing
Open to All — Chiphead Theater

4:00 PM – 4:45 PM

Encore Presentation: Optimizing Interconnect Through Application of Bayesian Optimization Utilizing 3D EM Solvers
Open to All — Mission City Ballroom B5

4:00 PM – 5:15 PM

Panel – PCIe6.0: Ingredients for Success
Open to All — Ballroom D

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9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

- D Drive World — Advanced Automotive
- E Embedded IoT World
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- General Event
- Special Event
- Sponsored Sessions

SESSIONS – THURSDAY, APRIL 7

4:00 PM – 5:15 PM

Panel – Test on Wheels: Test & Measurement for Automotive Standards
Open to All — Ballroom C

Panel – What is Needed for 224Gbps? System & Chip Vendors Perspective
Open to All — Ballroom H

4:15 PM – 4:35 PM

Deep Reinforcement Learning-based Channel-flexible Equalization Scheme: An Application to High Bandwidth Memory
Open to All — Chiphead Theater

4:40 – 5:00 PM

Risks & Enablers of Server Platform Design in Immersion Cooling
Open to All — Chiphead Theater

5:00 PM – 6:00 PM

Networking Session
Booth Bar Crawl
Open to All — Expo Floor

Sponsored by: Rosenberger Ansys

5:00 PM – 5:45 PM

Electrothermal Co-Simulation for PCB and Package Designs Using Celsius Thermal Solver
Open to All — Mission City Ballroom B5

TRACKS AND LEGEND

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1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement & Simulation Techniques for Analyzing Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

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Advancing High-Speed Communications with Industry-Leading Supplier, Amphenol at DesignCon 2022

By Suzanne Deffree, Group Event Director, DesignCon

As personal connectivity and IoT continue to expand, the broadband and telecom sectors are amid a significant surge in data consumption. As such, the cables and connectors market is experiencing high growth and market disruption, largely due to ballooning consumer demand for ultra-speedy 5G tech, increasing expenditure in enterprise cloud-based applications, and the rising pressure to improve bandwidth.

An industry poised to reach **$161.9 billion by 2025**, the cables and connectors sectors, like the high-tech interconnect, sensor, and antenna markets, are in critical need of peer-to-peer connection and education to overcome the challenges associated with such remarkable market performance and continue to innovate.

World-renowned supplier **Amphenol**, for example, is bolstering the refinement and delivery of new-age technology for end-to-end communications networks in today's connected world. As one of the industry's fastest growing organizations fueling innovation and meeting the demand for electronic systems performance, Amphenol is the host sponsor of **DesignCon**, the nation's largest event for chip, board, and systems design engineers.

The three-day conference and exhibition, to be held April 5-7 at the Santa Clara Convention Center, serves as the meeting place for the premier high-speed communications and system design conference, offering industry-critical engineering education in the heart of electronics innovation — Silicon Valley. Extending its opportunities beyond its 3-day in-person event, DesignCon this year will complement its event with an online component, where attendees can access select education and exhibitor resources pre- and post-event.

With DesignCon on the near horizon, DesignCon Group Event Director Suzanne Deffree spoke with Tom Pitten, Chief Technology Officer for Amphenol ICC. We discussed market trends, the upcoming event, and what attendees can look forward to learning about at the Amphenol booth.

Suzanne: What are the key industry growth drivers that will shape the industry's future, and how is Amphenol influencing these trends?

Tom: The most significant industry change over the last decade is the rise of the hyper-scale data center. These massive cloud computing centers now consume a substantial percentage of all electronic systems, and the hardware teams designing them have an insatiable appetite for performance and density. The vast array of leading-edge interconnect products Amphenol provides is helping to enable the rapid improvement in data center performance.

Suzanne: With the rapid advancement of technology, machinery and systems are becoming increasingly complex. How does Amphenol help its partners overcome this challenge while maintaining high performance and reliability?

Tom: The pace of development for higher performance, next-generation systems has clearly accelerated. The products that enable that performance are becoming exceedingly more complex and require innovative solutions in design and materials. To keep up with the pace, we're increasing our investment in enabling interconnect technologies years in advance from when they will be required. We're also dedicating more engineering resources to help lead industry standards by working closely with customers and collaborators.

Suzanne: We're so excited to have your support as DesignCon's host sponsor and a prominent exhibitor for this year's event. What excites you about reconnecting with your community in person this April?

Tom: We've been a participant at DesignCon since the early days in the mid-1990s. We've been thrilled to witness its incredible growth from a fledgling conference meant to advance industry knowledge of an emerging challenge called "Signal Integrity" to the premier conference on Electronic System Design. We're honored to be the host sponsor, and we're looking forward to the opportunity to connect in person with our customers and the entire electronics design community.

Suzanne: What role do you see DesignCon plays in advancing the system design engineering industry?

Tom: DesignCon has helped educate and continuously improve the engineering capability of the electronics industry. It continues to be an important avenue to share ideas and collaborate on new design challenges. We are looking forward to connecting with the industry and sharing new interconnect solutions from Amphenol.

Amphenol

EXHIBITOR LIST

Company	Booth
2J Antennas USA, Corporation	723
Accurate Circuit Engineering	855
Advanced Test Equipment Rentals	913
AGC Multi Material America, Inc.	954
Amphenol	833
Anritsu	1014
Ansys	1139
APCT	1445
Apex Semiconductors USA Co., Ltd.	523
Arcus Technology	610
Argosy Research Inc.	1455
Astera Labs, Inc.	524
Avishtech	635
Bellwether Electronic Corp	624
BizLink Special Cables Germany GmbH	1154
BizLink Technology, Inc.	1448
Cadence Design Systems, Inc.	927
CarlisleIT	1238
Circuit Foil Luxembourg	313
ColorChip	921
Corporate Ewaste Solutions	740
Co-Tech Development Corp.	319
Cvilux USA	712
Doosan Corporation Electro-Materials BG	718
DS SIMULIA CORP	1438
DVT Solutions, LLC	515
Electro Rent Corporation	1149
Elite Materials Co. Ltd. (EMC)	418
Ellisys	1022
EMA Design Automation Inc.	1243
EMQ.io	755
Epson America, Inc.	948
ept USA	958
eTopus Technology Inc	1255
evissaP	612
Flexible Circuit Technologies Inc	615
Fotofab, LLC	614
Genesis-Connected	912
Granite River Labs	622
Hirose Electric USA	1249
Hologram	750
Huber+Suhner	1054
Huwin	959

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Imagineering Inc.	619
Imec	752
In Compliance	742
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I-PEX	1441
Ironwood Electronics	519
Isola Group	743
ITEQ Corporation	315
JBC Tools USA, Inc.	1340
JPC Connectivity	834
Junkosha Inc.	1059
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Keysight Technologies	1039
KGS America Inc.	618
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Leeno Industrial Inc.	623
Lotes Co., Ltd	510
LPKF Laser & Electronics	1357
Luxshare-Ict	839
Malico Inc.	728
Marki Microwave, Inc.	1143
MathWorks	1338
Maury Microwave Corp	1264
Mouser Electronics	849
MultiLane	1155
Neoconix	419
Oak-Mitsui Technologies LLC	957
ODU-USA Inc.	613
Ohmega Technologies	955
OMDIA	1456
PacketMicro, Inc.	1345
PacTech	719
Paragon Innovations, Inc.	854
PFC Flexible Circuits	1344
Pico Technology	511
Plastronics	859
Polar Instruments	744
Polysciences Inc.	1262
Printed Circuit Engineering Association	1457
Qt Company	321
REGO-FIX USA	730
Rigol Technologies Usa	749

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RoBAT Ltd	1449
Rogers Corporation	518
Rohde & Schwarz USA, Inc.	1049
Rosenberger North America	1239
Samtec USA	939
Sanmina	733
Senko	1159
Siemens	949
Sierra Circuits, Inc.	818
Siglent Technologies Co., Ltd.	1254
Silitronics	832
Simberian, Inc.	915
Socionext America Inc.	1339
Somacis Inc.	527
Sonnet Software	1355
Southwest Microwave	714
Spectra7 Microsystems Ltd	1158
SRC Inc.	1343
Stäubli Electrical Connectors	521
Sumitomo Electric U.S.A.	1354
SureFire LLC	754
Surface Mount Technology Association	1342
SV Microwave	1439
SVTronics Inc	856
Swift Bridge Technologies	1012
Synergy Circuits Inc.	1358
Taiwan Union Technology Corporation	415
TDK - Lambda High Power Division	414
Technology Innovation Institute	748
TE Connectivity	819
Tektronix	827
Thistle Tech	756
TOYO INK AMERICA, LLC	412
TRAX Industrial Products	1263
TRS RenTelco	520
TSE	1259
US Conec, Ltd	1058
Versatile Power	421
Volex Inc.	1349
VPI Technology	919
withwave Co., Ltd	1163
Xpeedic Technology Inc.	727
Yamaichi Electronics USA	960

As Of 3/28/22

EXHIBIT HALL FLOOR MAP

EXHIBIT HOURS:

Wednesday, April 6
11:00 AM - 6:00 PM

Thursday, April 7
11:00 AM - 6:00 PM

- Wednesday Product Showcase Locations
- Thursday Product Showcase Locations
- Wednesday Booth Bar Crawl
- Thursday Booth Bar Crawl

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WEDNESDAY, APRIL 6, 2022

TIME	COMPANY	BOOTH
11:30 am	Rosenberger	1239
12:00 pm	ROHDE&SCHWARZ Make ideas real	1049
2:00 pm	Tektronix®	827
2:30 pm	samtec	939
3:00 pm	XPEEDIC ACCELERATE YOUR IC DESIGN	727
3:30 pm	ARGOSY®	1455

THURSDAY, APRIL 7, 2022

TIME	COMPANY	BOOTH
11:30 am	Rosenberger	1239
12:00 pm	ARGOSY®	1455

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DesignCon follows state and local guidance regarding protocols for attending large-scale events. Please check the event app and scan the below QR code for the most up-to-date information.

Visit DesignCon.com for up-to-date information regarding health & safety.

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WEDNESDAY, 5:00 – 6:00 PM

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THURSDAY, 5:00 – 6:00 PM

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AI is Getting Adopted Across Multiple Industries, from Healthcare to Aerospace.

By Suzanne Deffree, Group Event Director, DesignCon

The promise of artificial intelligence (AI) and machine learning (ML) is remarkable. There's no denying AI and ML have infiltrated nearly every industry, profoundly changing how technologists and engineers analyze today's seemingly endless vat of data and solving increasingly complex problems.

And it's everywhere. AI is widely used in healthcare, from supporting the sector's struggle against interoperability to forecasting disease. Aerospace engineers have been employing AI and ML technologies for years, enabling Mars exploration and fueling our curiosity to further explore the far reaches of space. And here on Earth, AI is enabling advancements toward autonomous driving.

Even though this revolutionary technology is transforming society, AI and ML elicit strong and emotional responses, unlike any other technology, due to unfamiliarity with automated and intelligent tools, inherent biases, and many other reasons. Advocates, such as renowned engineer **Laurence Moroney, Lead AI Advocate at Google** and keynote speaker at DesignCon, are spearheading the refinement and widespread education of AI and ML capabilities to propel the technology from its infancy into cross-industry maturation.

DesignCon, April 5-7 at the Santa Clara Convention Center, serves as the nation's largest event for chip, board, and systems design engineers and will re-unite this dynamic community for three days of education, networking, and deal-making, including an unmissable opening address by Laurence on April 6.

Suzanne: Could you speak to your role as Google's lead AI advocate?

Laurence: The main goal of advocates is to inform and inspire the community around the possibilities of technology and to bring the feedback and requirements of the community back to our company to ensure they're well understood. With that in mind, I run a team of people whose goal it is to do precisely that – and we achieve that through scalable means: blogs, social, videos, conference talks, etc. We also work on driving education curricula for Google and the world, including teaching MOOCs at universities and much more.

Suzanne: What challenges are you helping solve?

Laurence: The main challenge is to help people, organizations, companies, universities, governments, and more break through the hype cycle and understand what is possible with AI and Machine Learning. We do this through education and example, not by marketing our platform(s), but by truly helping people understand it from end to end, so they can ideate around how they may use it for their scenarios. That's one of the unique things about AI –when applied correctly, there can be solutions for just about any domain. Still, we have to have experts in that domain understand the technology so they can begin to work from a place of power in coming up with solutions.

Let me share one example – recently, I took part in an experiment with the cast and crew of a TV show to have an AI model create a script, and the actors would read through that script. This is much more difficult than it sounds when you understand the constraints – one of which was the availability of actors! Indeed, the four actors we used had never been in a scene before, so how could

an AI model create something for them? But it did, and the results were fascinating. Sometimes inspiring. Sometimes deep. Sometimes ridiculous, and always funny! None of these people were experts in AI, but one of them observed something that shows what I'm referring to earlier.

Given the nature of the TV show being a Sci-Fi one, it often used made-up words (aka 'technobabble'), and the AI model also ended up making up words. Some of these were quite funny, and they were all in context with the show. They sounded like the kind of thing you would see on the show. So, this actor realized that one of the hardest parts of his job is preparing for auditions. They can get hit with screen readings of difficult and made-up words, and they can't practice for that short of hiring a writer, which is prohibitively expensive. But with an AI model like this, he could have it create some, help him practice, and maybe pass the audition to get a new job! That's not something I or any other Googler would likely have thought of. But he did. And the same can happen in almost any field, so I want to help make that happen.

Suzanne: What opportunities are you breaking ground on?

Laurence: It's a continued effort to drive simplicity and awareness, and we continue to push hard in that direction. To that end, we continue to work hard to inform and inspire! Meanwhile, our research teams continue to push advances in machine learning to solve problems more easily, or faster, or cheaper, etc. In addition to that, there's ongoing effort into tools and services that make building responsible AI easier. Another thing I'm particularly passionate about – on the theme of widening access – is ensuring that people who don't have access to vast amounts of data can still have a solution that works on their smaller datasets. And of course, there's the continued push for simplifying the production deployment of AI from the huge scale in the Cloud, to the web, to the browser, the mobile device, the embedded system, and all the way down to the microcontroller!

Suzanne: How can design engineers today better embrace the promise of AI?

Laurence: By investing in understanding how it works, they can maximize the benefits of the technology and platforms. Additionally, how they can operationalize around AI models – training the model is just the end of the beginning. After that, there's deployment, managing, updating, and keeping a continuous cycle there while doing it all responsibly!

Suzanne: You are a keynote speaker at DesignCon. What can attendees look forward to learning in your presentation?

Laurence: No Spoilers! Just kidding – the talk title is "Cutting through Hype and moving to Production: the realities of AI and Machine Learning" – and that's what I want to drill down into – understanding the hype cycle and how to navigate through it, and then using that to demonstrate some of the possibilities once you understand the underlying technology and how it works. It'll have plenty of stories of people who broke through that and came up with novel solutions that nobody would have thought of before AI and ML because they were prohibitively difficult or expensive! Hopefully, that will help you apply this type of thinking to your domain, and from there, come up with something new and exciting that changes your world!

Suzanne: What excites you most about re-connecting with your community face-to-face at DesignCon this April?

Laurence: The last time I spoke with a large, live audience was at the beginning of 2020, when we were just beginning to understand the pandemic. Since then, I've been sitting in my office speaking to a webcam when I do presentations. I'm really excited for the dynamics of a live audience and those moments of inspiration when the proverbial penny drops during a conversation and people begin to unlock what they'll be able to achieve using AI and ML. That's one of my favorite moments, and I hope DesignCon has many!

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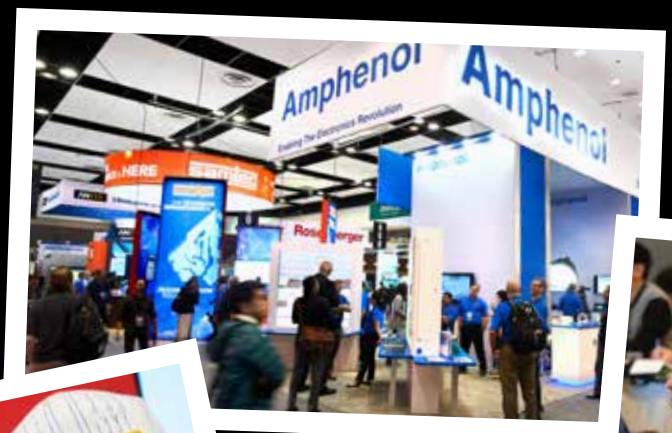

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Women in Autonomy

Wednesday, April 6, 2022 | 10:00 am | Elizabeth A. Hangs Theater

Each year DesignCon recognizes outstanding contributions to the educational goals of the DesignCon program.

The Best Paper Awards serve to acknowledge the authors who receive them as leading practitioners in semiconductor and electronic design.

Congratulations to the 2021 award winners:

2021 Best Paper Award Winners

"A Case Study in the Development of a 112 Gbps-PAM4 Silicon & Connector Test Platform"

"Cost Effective Power Integrity Methodology for Integrating Next-Generation High-Speed IPs"

"End-to-end IBIS-AMI Modeling & Simulations of Electrical/Optical Links"

"From Simulation to Production: An In-Depth Look at Designing & Productizing GDDR6x, the World's First PAM-4 Memory Interface"

"Global Optimization of Wireline Transceivers for Minimum Post-FEC vs. Pre-FEC BER"

"Holistic Power Supply Induced Jitter Accumulation Response Surface Modeling for HBM Chiplet Interconnect System"

"Innovative Designs for Optimizing 112G+ BGA Fan-Out & Connector Footprint Crosstalk"

"Neural Language Model Enables Extremely Fast & Robust Routing on Interposer"

"SNDR Analysis & Its Impacts on Link Performance"

2021 Early-Career Best Paper Award Winner

"Analysis of Electro-Static Discharge to Through-Silicon Via"

Thursday, April 7, 2022 | 10:00 am | Elizabeth A. Hangs Theater

The winner will be selected based on his or her leadership, creativity, and out-of-the-box thinking brought to design/test of chips, boards, or systems, with particular attention paid to areas of signal and power integrity.

Congratulations to these four exceptional finalists:
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Richard Mellitz, Distinguished Engineer, Samtec
Steve Sandler, Founder, Picotest.com
Lambert (Bert) Simonovich, Founder, Lamsim Enterprises

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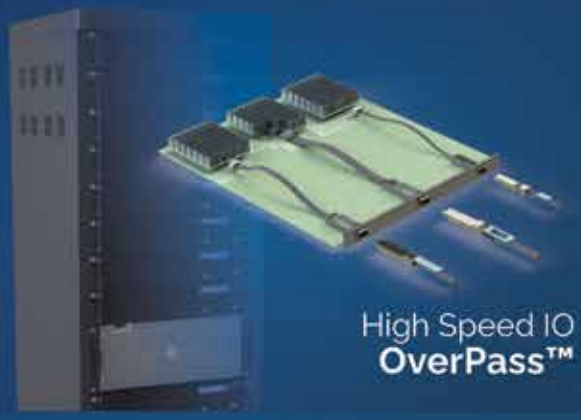

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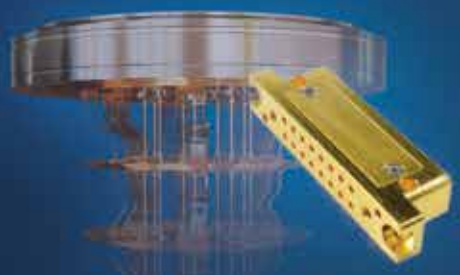

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