DesignCon® Digital
WHERE THE CHIP MEETS THE BOARD

OCTOBER 5 & 6, 2021 — AGENDA AT A GLANCE

TUESDAY, OCTOBER 5, 2021 *Programming Note: All Times Are PT*

9:00 AM — 9:45 AM | Keynote: The Keys to Innovation: Priming Your Brain to Percolate Brilliant Ideas
The route from problem to solution is a swirling path with Aha! moments lighting the way. In this presentation, we examine the neural processes that percolate insights into consciousness: the physics of lateral thought, the power of perspective, the value of novelty, and how your brain selects and rejects ideas before you're even aware of them. Then we turn to methods that can prime our brains to solve the challenges that we face as individuals as well as those that we face together.
Speaker: Ransom Stephens, Ransom's Notes, Owner
Session Type: Keynote Address

9:45 AM — 10:30 AM | FRA & VNA Frequency Domain Measurements in an Oscilloscope
This session will cover the differences between Frequency Response Analysis (FRA) and Vector Network Analysis (VNA) measurements. These common industry names are misleading, since FRA is a VNA measurement, but there are very significant differences between the two. Most Oscilloscope manufacturers now offer conventional Control Loop Gain and PSRR measurements. There are much more exciting applications beyond those conventional measurements and while we will discuss those, the session will be much more focused on what lies beyond them.

We'll discuss the differences between FRA and VNA measurements and present a wide variety of examples for each measurement type. We'll show how they are performed in a modern oscilloscope and when it may not only be possible but may be the best instrument choice.

We'll talk about the pros and cons and share some of the best tips for getting the absolute best measurement results.
Speaker: Steve Sandler, Picotest, Managing Director
Session Type: Conference - SI/PI Track

9:45 AM — 10:30 AM | Hidden Secrets of IBIS Sampling Specifications
The I/O Buffer Information Specification-Algorithmic Modeling Interface (IBIS-AMI) enables sharing of a model, which encompasses the complexity of the transmitter and receiver blocks. The IBIS-AMI model outputs an equalized waveform along with sampling information to the EDA tool. This paper gives an overview on sampling through the AMI_Init and AMI_GetWave flow part of the IBIS specification along with insight into reserved parameters usage. Results through seven EDA tools in modelling three different sampling mechanisms show the importance of sampling information when modelling through the IBIS specification. This is an attempt to make model developers and model users aware of the importance of sampling when running channel simulations.
Speaker: Todd Bermensolo, Keysight Technologies, Application Engineer
Speaker: Hansel Dsilva, Achronix Semiconductor Corporation, Staff Signal Integrity Engineer
Session Type: Conference - Automotive Track

9:45 AM — 10:00 AM | Thought Leader: Mark Wehde
Mark Wehde of the Mayo Clinic shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Mark Wehde, Mayo ClinicChair, Division of Engineering
Session Type: Thought Leader Interview

10:00 AM — 10:45 AM | A SI Engineer's Guide to Successful GDDR6 Design
Speaker: Celso Faia **Speaker:** Brad Griffin
Session Type: Tech Theater

10:30 AM — 11:15 AM | Communication Link Modeling Using PyBERT
This session will cover serial communications link modeling and equalization optimization, using the public domain, open source tool: PyBERT (https://github.com/capn-freako/PyBERT/wiki). We will target our optimization efforts at the new OCP ODSA-BoW interface, including crosstalk.
Speaker: David Banas, Luminous Computing, Senior Fellow
Session Type: Conference - SI/PI Track

10:30 AM — 11:15 AM | The Future of Automated Driving
Speaker: Phil Magney, VSI Labs, Founder & President
Session Type: Conference - Automotive Track

10:45 AM — 11:00 AM | Thought Leader: Ken Wyatt
Key Wyatt of the Wyatt Technical Services shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Ken Wyatt, Wyatt Technical Services LLC, Sr. EMC Engineer
Session Type: Thought Leader Interview

11:00 AM — 11:45 AM | Emerging Compute Architectures for the Evolving Data Center
As the world has become increasingly connected, processing continues to evolve from the familiar cloud computing paradigm. The vast profusion of IoT devices has contributed to the exponential rise in data volume. Greater intelligence is moving to the edge of the network and to the end points themselves to provide greater, real-time functionality. The implications for global network infrastructure are profound and there are significant developments in computing architectures which will shape the future data center.
Speaker: Steven Woo, Rambus, Fellow and Distinguished Inventor
Session Type: Tech Theater

11:45 AM — 12:00 PM | Thought Leader: Paul Pickering
Paul Pickering of Omdia shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Paul Pickering, Omdia, Senior Research Analyst, Power Semiconductors
Session Type: Thought Leader Interview

12:00 PM — 12:45 PM | Electromagnetic Fields for Normal Folks
The material presented will be focused on the physics of electromagnetic energy basic principles, presented in easy to understand language with plenty of diagrams. Attendees will discover how understanding the behavior of EM fields can help to design PCBs that will be more robust and have better EMC performance. This is not rocket science, but an easy to understand application of PCB geometry.
Speaker: Dan Beeker, NXP, Senior Principal Engineer
Session Type: Conference - PCB Track

12:00 PM — 12:45 PM | Getting Started with Multicore Microcontroller Applications
The IoT and ML applications are driving developers to leverage multicore microcontroller solutions in order to meet performance, real-time and energy requirements. The most common multicore microcontroller solution is currently asymmetric processing in which the microcontroller contains two difference cores. This presents a developer with many potential solutions for their application.

In this session, we will explore how to get started with multicore applications. We will examine different design patterns for partitioning the application, how to use an RTOS in a multicore environment and introduce developers to the AMP framework. Examples will be provided for a commonly available development board.
Speaker: Jacob Beningo, Beningo Embedded Group, President
Session Type: Conference - 5G/IoT Track

12:00 PM — 12:15 PM | Thought Leader: Cathy Liu
Cathy Liu of Broadcom shares her engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Cathy Liu, Broadcom Inc., Distinguished Engineer and Director – Broadcom SerDes Architecture and Modeling Group
Session Type: Thought Leader Interview

12:15 PM — 12:30 PM | Thought Leader: Chris Cheng
Chris Cheng of Hewlett Packard Enterprise shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Chris Cheng, HP Enterprise, Distinguished Technologist
Session Type: Thought Leader Interview

12:45 PM — 1:30 PM | New Design & Testing Challenges in Flexible Electronics
Reliability data and test protocols are critical to the product design process, which are influenced by test levels, duration and various environmental acceleration factors. All flexible electronics components, require long-run repeatable mechanical deformation testing such as flexing in hostile conditions to determine failure analysis used to assess new failure modes such as delamination, buckling and contact failures. Previously engineers used, universal testers only measured the physical limits of material properties, e.g., until it broke; or built their own tools which were not adequate for mechanical precision, long cycle runs nor scalability across different organizations.

Since 2016, Bayflex Solutions has worked with the many branded devices and their supply chains. In this session we will cover the various specific testing challenges and insights such as various mechanical testing, optical imaging software and hostile environments, gained from developments in designing the latest smartphones, wearables and display devices.
Speaker: Eisuke Tsuyuzaki, Bayflex Solutions, Founder
Session Type: Conference - PCB Track

12:45 PM — 1:30 PM | 5G & Edge Compute in the Metaverse: What it Means for the Future of UI & UX
Speaker: Joshua Ness, Verizon 5G Labs, Sr Manager
Session Type: Conference - 5G/IoT Track

12:45 PM — 1:00 PM | Thought Leader: Steven Woo
Steven Woo of Rambus shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Steven Woo, Rambus, Fellow and Distinguished Inventor
Session Type: Thought Leader Interview

1:00 PM — 1:45 PM | Selecting the Right High-Performance Memory Solution
An exponentially rising tide of data has led to the development of application-specific silicon to tackle the requirements of demanding workloads such as AI/ML training, Advanced Driver Assistance Systems (ADAS) for automotive, network graphics and HPC. To keep these processors and accelerators fed requires state-of-the-art memory solutions that deliver extremely high bandwidth. Frank Ferro will discuss design and implementation considerations of HBM2E and GDDR6 memory subsystems to address the bandwidth needs of next-generation computing applications.
Speaker: Frank Ferro, Rambus, Senior Director of Product Management
Session Type: Tech Theater

1:30 PM — 2:15 PM | 3D Packaging Solutions
3D packaging promises benefits including continued performance scaling and higher bandwidth connections between chips. In order to realize these benefits expertise in power integrity (PI), signal integrity (SI), interposer design and system-level simulation are required. This presentation will cover the design considerations and methodologies for successfully implementing a 3D package design for an HBM2/HBM2E solution.
Speaker: Ming Li, Rambus, Technical Director
Session Type: Tech Theater

1:45 PM — 2:00 PM | Thought Leader: Daniel Beeker
Dan Beeker of NXP shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Daniel Beeker, NXP, Senior Principal Engineer
Session Type: Thought Leader Interview

WEDNESDAY, OCTOBER 6, 2021 *Programming Note: All Times Are PT*

9:00 AM — 9:45 AM | Keynote - Autonomous Vehicle Technology: Sensing What Matters
Autonomous and automated vehicles are coming to a road near you, and whether it's a truck, car, train, or delivery bot, it's a moving machine that will need to intelligently sense and safely navigate its surroundings. What is the current market for autonomous vehicles, what are the growth drivers, and how does the industry solve the most challenging edge cases inhibiting broader rollouts? In this presentation, recorded at DesignCon 2021, AEye Director of Product Management Indu Vijayan discusses AI-driven sensing and how that technology is helping vehicles see smarter, respond faster, and accelerate adoption of autonomous features.
Speaker: Indu Vijayan, Director of Product Management, AEye
Session Type: Keynote Address

9:45 AM — 10:30 AM | Considerations for Reference Equalizer Optimization at 112Gbps
The application of compound equalizer structures in various emerging DataCom standards presents a new set of requirements with regards to how reference receiver tap settings are configured. This paper will review advances in "tuning" multi-gain-stage linear equalizers and decision feedback equalizers operating serially. The goal of the standards methodology modeled around MMSE or Mueller-Muller techniques is not to "over-tune" the equalizer structures but to define a balanced methodology which can be implemented uniformly by test equipment vendors. It reduces the sensitivity to measurement equipment and test conditions and leaves the receiver designer some margin to further improve on. Similar widely supported approach can be found with dual-dirac method of jitter decomposition where tradeoff between various jitter components is left for the designer. Additionally, the process of tuning two separate equalizer structures can lead to error propagation stability problems if to much weight is placed on one equalizer. Several methods will be reviewed in the context of equalization performed for IEEE 802.3ck C2M 100Gbps specifications.
Speaker: John Calvin, Keysight Technologies, Senior Solutions Planner, IP Wireline Planner
Session Type: Conference - T&M/EMI Track

9:45 AM — 10:30 AM | Design Case Study & Experimental Validation for a 100 Gb/s Per Lane C2M Link Using Channel Operating Margin
The Chip-to-Module (C2M) interface as specified by the IEEE 802.3 Standard Working Group, and currently being updated for higher data rates, implements links that must perform up to 800 Gb/s (8 × 100 Gb/s) within the internet infrastructure physical layer. The design of these channels requires multiple engineering disciplines that fused together to create a comprehensive workflow. The standard measurements and specifications such as insertion loss, return loss, crosstalk, impedance profile and eye diagram may be no longer sufficient to ensure compliance as well as interoperability. The Channel Operating Margin (COM) is an emerging Figure of Merit (FOM) that incorporates all active and passive components within the channel to allow performance trade-offs to be made by designers.

While COM is a voltage signal to noise ratio, the C2M uses another related figure of merit, the Voltage Eye Closure (VEC), which is the ratio of eye opening to the amplitude of the electrical output. Since the eye opening is the complement to noise VEC it is directly computable from COM and vice versa.

Moving higher and higher in the data rate poses challenges to the applicability of COM/VEC computation for a channel performance design and interoperability compliance evaluation. This paper will characterize a C2M link using advanced simulation and measurement tools to validate the applicability of the design solution explored by COM algorithms. This will confirm its effectiveness without the need to continuously rely on complex, time consuming and expensive measurements, whenever approaching a new C2M channel design.

A typical physical layer channel design, including simulation, measurements and debug, identifies specific challenges with its subsequent potential solutions evaluated by COM.
Speaker: Mike Resso, Keysight Technologies, Signal Integrity Application Scientist
Speaker: Rick Rabinovich, Keysight Technologies, Signal Integrity Distinguished Engineer
Session Type: Conference - Connectivity/Interconnects Track

9:45 AM — 10:00 AM | Thought Leader: Frank Ferro
Frank Ferro of Rambus shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Frank Ferro, Rambus, Senior Director of Product Management
Session Type: Thought Leader Interview

10:00 AM — 10:45 AM | Introduction to PCI Express 6.0 Interface Solutions
The latest generation of the PCI Express, PCIe 6.0, advances performance to 64 GT/s in support of advanced workloads and networking. In this presentation, PLDA technology expert Trupti Gowda discusses the changes upcoming in PCI Express 6.0 solutions including the transition to PAM4 signaling and low latency forward error correction (FEC).
Speaker: Trupti Gowda, PLDA Inc, Field Application Engineer
Session Type: Tech Theater

10:30 AM — 11:15 AM | Two Novel Skew Compensation Techniques for Reducing Mode Conversion
Two techniques for intra-pair length matching of differential routing are proposed: Asymmetrical Dual Bend(ADB) and Hybrid U-Turn(HUT), in order to reduce the differential mode to common mode conversion in system. These layout techniques help in achieving lower EMI without impacting SI performance and with insignificant effect on PCB cost.

1. Four types of Asymmetric Dual Bend(ADB) designs are evaluated in this presentation by simulating the EMI and SI performance. The results illustrate that the asymmetric dual bend scheme can provide 10+ dB improvement for Scd21 in stripline layout and nearly 5dB improvement for microstrip layout, while no impact on SddSeveral PCB coupons were also made, and the results match quite well between simulation and measurement.

2. Hybrid U-Turn(HUT) is proposed in this presentation for intra-pair length matching as well as inter-pair skew simultaneously by introducing two different kinds of corners. The simulation results show nearly 10dB improvement in Scd21 and PCB coupon measurement also verify the performance.

Speaker: Jianquan Lou, Cisco System, EMC engineer
Session Type: Conference - T&M/EMI Track

10:30 AM — 11:15 AM | Effect of the Maximum Frequency & Frequency Resolution of S Parameters on Channel Simulation
For reliable and accurate system modelling of OIF CEI-112G XSR and VSR links accurate channel representation is paramount. Channels are usually measured or simulated in the frequency domain with certain resolution frequency, fres, and up to a maximum frequency, fmax. As baud rates continually increase, fres and fmax are generally limited by measurement instrumentation and/or computational resources. From a practical point of view, a channel is assembled via the cascade of different components (traces, packages, connectors, etc.) that may be characterized using different fres and fmax values. In this paper, we investigate the effect of such limitations on the overall system characterization. It is shown via theory and numerical analysis of a typical 112G XSR channel how fmax and fr can severely result in unreliable, sometimes unobvious, channel simulation results. We provide rules of thumbs and possible remedies. An important aim of this work is to highlight that the impact of the limitations is of a fundamental nature and may add significant artifacts that influence the decisions of the signal integrity engineer.
Speaker: Sameh Elnaggar, Semtech, Staff Engineer
Session Type: Conference - Connectivity/Interconnects Track

10:45 AM — 11:00 AM | Thought Leader: Indu Vijayan
Indu Vijayan of AEye shares her engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Indu Yijayan, AEye, Director of Product Management for ADAS Solutions
Session Type: Thought Leader Interview

11:00 AM — 11:15 AM | Thought Leader: Brad Griffin
Brad Griffin of Cadence shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Brad Griffin
Session Type: Thought Leader Interview

11:15 AM — 11:30 AM | Thought Leader: John Blyler
John Blyler of Design News shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: John Blyler, Design News, Senior Editor
Session Type: Thought Leader Interview

11:15 AM — 12:00 PM | Hyperlabs Presentation
Speaker: Brian Doxey
Session Type: Conference T&M/EMI

11:15 AM — 12:00 PM | Introduction to CXL 2.0 Interconnect Solutions
Compute Express Link (CXL) has evolved rapidly since its launch in 2019 and is slated for debut in the next generation of server platforms coming in 2022. Building on the same physical layer as PCI Express, CXL offers memory cache coherency enabling new use models of memory expansion and memory pooling offering improved server performance and TCO. Join PLDA technology expert Trupti Gowda for a discussion of key features and implementation details for CXL interconnects.
Speaker: Trupti Gowda, PLDA Inc, Field Application Engineer
Session Type: Tech Theater

11:45 AM — 12:00 PM | Thought Leader: Bill Hargin
Bill Hargin of Z-zero shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Bill Hargin, Z-zero, Director of Everything
Session Type: Thought Leader Interview

12:00 PM — 12:45 PM | Northrop Grumman Case Study: Rigorous Design Analysis of a DDR4 DIMM-Based System
This session will review multi-board simulation model with custom ASIC, MCM package, PCBA, UDIMM and RDIMM models.
Speaker: Ben Dannan, Northrop Grumman, Staff Digital Engineer
Session Type: EDA/Modeling/Simulation

12:00 PM — 12:45 PM | What's Next for High-Bandwidth Memory?
With the insatiable need for higher bandwidth in state-of-the-art AI/ML training, the HBM standard will continue to evolve beyond 4 Gbps performance achieved in HBM2E. Memory interface technology expert, Frank Ferro will discuss design considerations and enabling technology for the next generation of high-bandwidth memory.
Speaker: Frank Ferro, Rambus, Senior Director of Product Management
Session Type: Tech Talk

12:45 PM — 1:30 PM | A Case Study in the Development of a 112Gbps-PAM4 Silicon & Connector Test Platform
The continued progression to higher data rates puts increasing demands on the design of practical serdes channels. At 112G-PAM4, the UI is only 17.86ps, and signal transmission in the PCB must be highly optimized for loss, reflections, crosstalk and power integrity. This paper will describe the signal-integrity and power-integrity design process, show simulated SI and PI performance correlated to measured data as well as measured eye diagrams of a test board that uses a 112G-capable silicon and high-speed compression-mount cable connectors. The resulting test channel aims to meet the toughest reference test fixture insertion loss requirements of IEEE P802.3ck-100Gb/s and OIF CEI-112G PAM4 specifications.
Speaker: Jean-Remy Bonnefoy, Samtec, Systems Engineer
Session Type: Conference - EDA/Modeling/Simulation Track

12:45 PM — 1:00 PM | Thought Leader: Michael Yang
Michael Yang of Omdia shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Michael Yang, Omdia, Senior Director, Semiconductors
Session Type: Thought Leader Interview

1:00 PM — 1:15 PM | Thought Leader: Maria Agoston
Maria Agoston of Tektronix shares her engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Maria Agoston, Tektronix, Principal Engineer
Session Type: Thought Leader Interview

1:15 PM — 1:30 PM | Thought Leader: Sang Oh
Sang Oh of Omdia shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Sang Oh, Omdia, Senior Research Analyst, Automotive Semiconductors
Session Type: Thought Leader Interview

1:45 PM — 2:00 PM | Thought Leader: Phil Magney
Phil Magney of VSI Labs shares his engineering insights and experience in an exclusive one-on-one conversation with DesignCon.
Speaker: Phil Magney, VSI Labs, Founder & President
Session Type: Thought Leader Interview