DesignCon® 2021

WHERE THE CHIP MEETS THE BOARD

SAN JOSE MCENERY CONVENTION CENTER
SAN JOSE, CA

CONFERENCE:
AUGUST 16 – 18, 2021

EXPO:
AUGUST 17 – 18, 2021

Register at DesignCon.com / #DesignCon

informa markets

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Joining DesignCon In 2021…

Drive WORLD CONFERENCE & EXPO | esc EMBEDDED SYSTEMS CONFERENCE

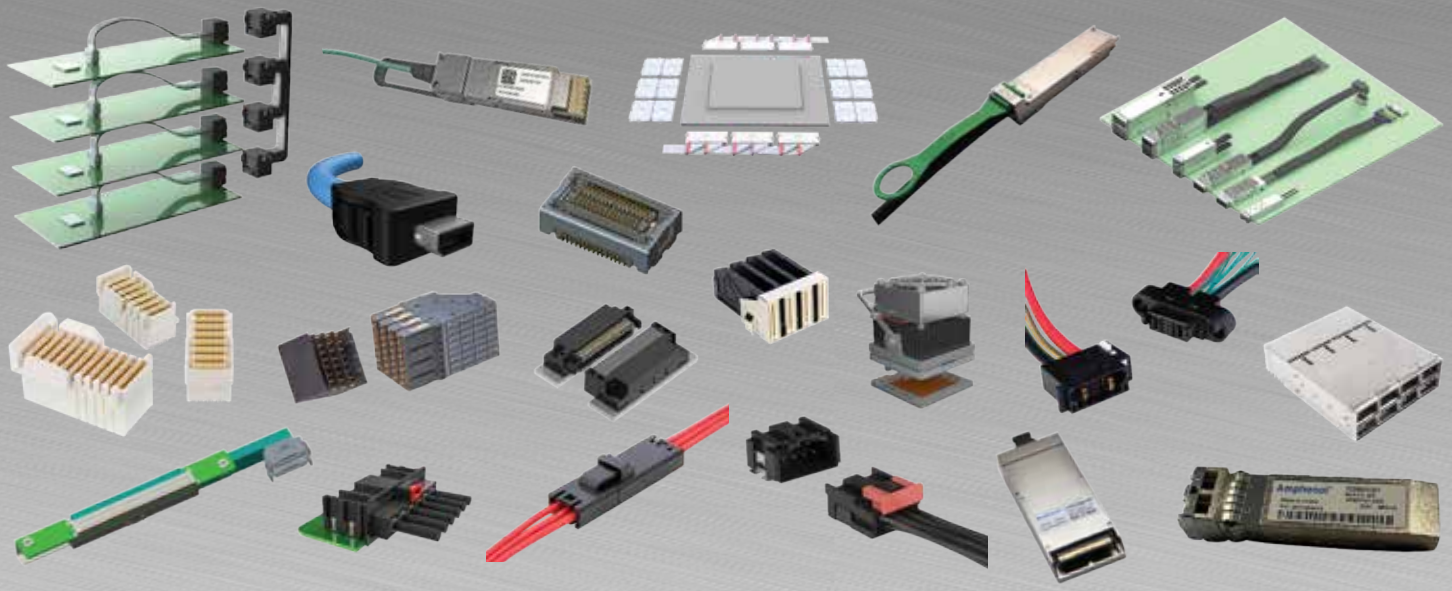
Drive World+Embedded Systems Conference (ESC)

August 16 – 18, 2021 / San Jose McEnery Convention Center

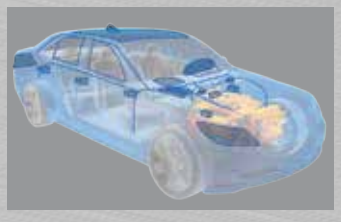
Register at DriveWorldExpo.com

Amphenol

Come visit us to discuss your Interconnect needs

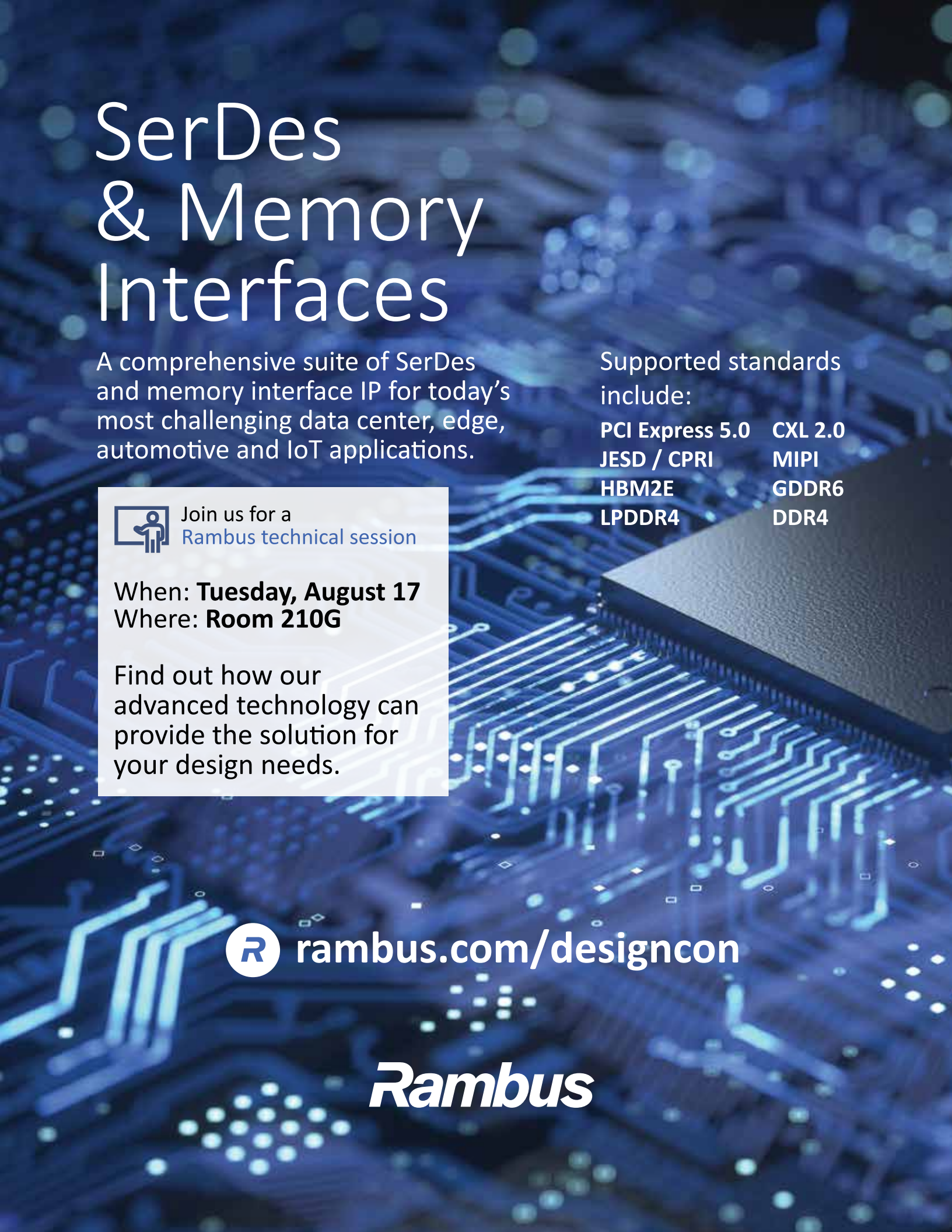


Enabling the Electronics Revolution in your markets



Check out our live demonstrations

Booth #707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DDR4
Join us for a Rambus technical session
When: Tuesday, August 17
Where: Room 210G
Find out how our advanced technology can provide the solution for your design needs.
rambus.com/designcon
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DESIGNCON® 2021
WHERE THE CHIP MEETS THE BOARD

WELCOME TO DESIGNCON

Welcome back. It's been a while and it's so good to say hello again.

The world has changed a lot since we last gathered at DesignCon in January 2020, but what hasn't changed is the need for education and sourcing to drive tomorrow's innovations today. And we're here for that.

Over the course of the in-person event, you'll find more than 150 sessions presented by 155 speakers, 3 visionary keynotes offering a look at what's coming next, 85 leading suppliers ready to help you design, and multiple networking opportunities to help you re-connect with your peers, customers, tech influencers, and friends.

This year at DesignCon we welcome Drive World+ESC (Embedded Systems Conference), adding more focus on topics that have been in high demand among our DesignCon community including, IoT, embedded hardware/software, and automotive electronics and intelligence. Conference pass holders will find Drive World+ESC sessions in the schedule and all pass holders can stop by the expo for live sensing demos on two advanced vehicles, presented by the expert engineers at VSI Labs.

Be it through demos, education, or sourcing, the week is all about helping you engineer. If there's an area you want to sharpen your design skills in, be sure to search DesignCon's full education schedule at DesignCon.com by theme. You'll find helpful breakouts on popular topics like 5G, consumer electronics, data centers, high-speed communications, and more. DesignCon's smart phone app also offers exhibitors sorted by categories like analog/mixed signal, components, signal integrity, test and measurement equipment, and more to help you find the tech you need.

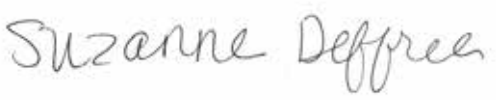
And make some time to focus on your career, too, over the coming days. Check out the 2021 Career Zone on the expo floor for networking on topics like advancing emerging engineers, technical paper writing tips, and women and minorities in STEM. And be sure to take advantage of tools being offered in the space—including one-on-one salary negotiation advice and professional headshots—to help take your career to that next level.

Enjoy DesignCon 2021, partnered with Drive World+ESC, and be sure to take advantage of all we have to offer this week. Know that in all our planning, health and safety have been a top priority. Visit DesignCon.com for health and safety information and watch for reminders at the event throughout the week.

On behalf of DesignCon and Informa Markets—Engineering, thank you to all of our speakers, committee members, sponsors, exhibitors, attendees, and partners who help bring this week to engineers.

We look forward to re-connecting with you August 16-18, 2021.

See you at the San Jose McEnery Convention Center!



Suzanne Deffree
Group Event Director, DesignCon and Drive World+ESC

informa markets
Engineering

KEYSIGHT TECHNOLOGIES

Accelerate Your Fastest Digital Designs

EDUCATION FORUM

PCIe6, 400G/800G,
Next-Gen Type-C,
Power Integrity,
Signal Integrity,
Fronthaul Network

San Jose McEnery
Convention Center, 210E

Tues. August 17, 8:30 am -12:45 pm
Wed. August 18, 8:30 am - 12:45 pm

Visit Booth #807

DESIGNCON® 2021

WHERE THE CHIP MEETS THE BOARD

FAMILY REUNION

Welcome Reception

Monday, August 16, 2021
6-8 pm | Outdoor Plaza at the Idea Tree

Sponsored by:

samtec

Enjoy complimentary cocktails, picnic-themed foods, lawn games and more!

Open to all DesignCon and Drive World+ESC attendees, exhibitors, speakers, media and TPC.
(Badges required for entry.)

TPC MEMBERS

We would like to thank the volunteers who served on the Technical Program Committee (TPC) for DesignCon 2021. Their contributions as reviewers of the abstracts and papers have made it possible for us to maintain the DesignCon standard of excellence and deliver an outstanding program again this year.

Brice Achkir*, Distinguished Eng./Sr. Eng. Director, Cisco Systems
Joseph Aday*, Sr. Member of Technical Staff, Lockheed Martin
Maria Agoston*, Principal Engineer, Tektronix
Ravinder Ajmani, Technologist, Electronic Design Engineering, Western Digital
John Andresakis, Technical Marketing Leader, DuPont
Yianni Antoniades, Senior Electrical Engineer, Winchester Interconnect
Bruce Archambeault, Retired
Pervez Aziz*, Senior Principal Engineer, Nvidia
Seungyong (Brian) Baek, SI Architect, Apple
Nitin Bhagwath, Principal Technical Product Manager, Mentor Graphics, a Siemens Business
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Heidi Barnes*, SI/PI Applications Engineer, Keysight Technologies
Josiah Bartlett, Principal Engineer in Asics and Technology Organization, Tektronix
Dale Becker, Distinguished Engineer, IBM
Wendem Beyene*, Principal Engineer/Manager, Programmable Hardware Engineering, Intel
Luis Boluna, Sr. Application Engineer, Keysight Technologies
David Brunker, Technical Fellow, Molex
Robert Carter*, Vice President of Technology and Business Development, Oak-Mitsui Technologies
Chris Cheng*, Distinguished Technologist, HP Enterprise
David Choe, Principal Applications Engineer, Cadence
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Tom Cohen, Principal Engineer, Amphenol
Davi Correia, Sr. Principal Application Engineer, Cadence Design Systems
O.J. Danzy, Senior Application Engineer, Keysight Technologies
Jan De Geest, Senior Staff R&D Signal Integrity Engineer, Amphenol
Jay Diepenbrock, Consultant, SIRF Consultants
Vladimir Dmitriev-Zdorov, Principal Engineer, Mentor Graphics, a Siemens Business
Greg Edlund, Senior Engineer, IBM
Jason Ellison*, Sr. Staff Signal Integrity Engineer, Amphenol
Paul Franzon, Cirrus Logic Distinguished Professor, Director of Graduate Programs, NCSU
Sanjeev Gupta*, R&D Manager, Intel
Sunil Gupta, SIPI Technical Lead, Qualcomm Technologies
Robert Haller*, Sr. Principal Hardware Engineer, Extreme Networks
Gert Havermann, Signal Integrity Engineer, HARTING
Allen F. Horn III*, Research Fellow, Rogers
Rockwell Hsu, Technical Leader, Cisco Systems
Seunghyun Hwang, Principal Engineer, Nvidia
Namhoon Kim, Chip Package Design Architect, Google
Beomtaek Lee, Sr. Principal Engineer, Intel
Mike Li*, Fellow, Intel
Zhe Li, Hardware Engineer, Google
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Chris Loberg*, Marketing Manager, Tektronix
Om Mandhana, Staff Services AE, Cadence Design Systems
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Jon Martens, Fellow, Anritsu

TPC MEMBERS

Mehdi Mechaik*, Sr. Signal Integrity Engineer, Amazon Lab126
Ted Mido, Principal R&D Engineer, Synopsys
Martin Miller, Chief Scientist, Teledyne LeCroy
Akshay Mohan, EM Technology Lead, Amazon Lab126
Jose Moreira*, Senior Staff Engineer, Advantest
Zhen Mu*, Product Engineering Architect, Cadence Design Systems
Riaz Naseer, Staff Signal Integrity Engineer, Ciena
Alfred P. Neves*, Chief Technologist, Wild River Technology
Istvan Novak*, Principal Signal and Power Integrity Engineer, Samtec
Dan Oh, Vice President, Samsung
Vishram Pandit*, Technology Lead (Signal/Power Integrity), Intel
Jongbae Park, System SI Architect, Apple
Pete Pupalaikis, VP, Technology Development, Teledyne LeCroy
Kelvin Qiu, Senior Signal Integrity and Power Integrity Engineer, Google
Fangyi Rao, Master Engineer, Keysight Technologies
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Masashi Shimanouchi, Design Engineer, Intel
Yuriy Shlepnev, President, Simberian
Ben Silva, Analog Engineer, Intel
Bert Simonovich, President, Lamsim Enterprises
Chad Smutzer, Senior Engineer, Mayo Clinic
Mike Steinberger, Lead Architect, Serial Channel Products, SiSoft
Ransom Stephens*, Signal Integrity Sage, Ransom's Notes
Changyi Su, Staff Design Engineer, Xilinx
Suresh Subramaniam, Principal Engineer/Architect, Xilinx
Madhavan Swaminathan, John Pippin Chair Professor in Microsystems Packaging & Emag, Georgia Tech
Donald Telian, Owner/Consultant, SiGuys
Lars Thon*, Consultant, LT Engineering
Thomas To*, Director, Xilinx
Peter Tomaszewski, Sr Field Applications Engineer, Tektronix
Ambrish Varma*, Sr. Principal Software Engineer, Cadence Design Systems
Harald von Sosen, Principal Engineer, Mentor, A Siemens Business
Juan Wang, Senior Staff Engineer, Xilinx
Scott Wedge, Principal Engineer, Synopsys
Todd Westerhoff*, Product Marketing Manager, Mentor, A Siemens Business
Markus Witte, Systems Engineer, Grimme
Randy Wolff, Principal Signal Integrity Engineer, Micron Technology
Hsinho Wu*, Design Engineer, Intel
Ken Wu, Hardware Engineering Manager, Google
Chris Wyland*, Sr. Staff Engineer, Juniper Networks
Kai Xiao, Principal Engineer, Intel
Mobashar Yazdani*, Strategic Semiconductor Manager, Google
Iliya Zamek, Architect, Technical Manager, HCL America
Geoffrey Zhang, Distinguished Engineer and Supervisor, Xilinx
Pavel Zivny, Domain Expert, Tektronix

*2021 track co-chair

EXHIBITOR ADVISORY COMMITTEE

A special thank you to the DesignCon 2021 Exhibitor Advisory Committee (EAC) who show dedication to DesignCon and assist with efforts to maximize the exhibiting experience for all participating suppliers.

Lorri Bupp, Marketing Specialist, Amphenol
Jennifer Chausse, Field Marketing Manager, Mentor, A Siemens Business
Harry Christie, VP of Sales, Gigatest Labs
Deanne Deville, Events Manager, Socionext America
Verly Flores, Field Marketing Manager, Cadence Design Systems
Thomas Hudak, Marketing Communications Manager, Tektronix
Hilary Lustig, Marketing Communications Manager, Teledyne LeCroy
Yuriy Shlepnev, President, Simberian Inc.
Eriko Yamato, Marketing Manager, Oak-Mitsui Technologies

EMERGING ENGINEER COMMITTEE

Thank you to the members of the DesignCon 2021 Emerging Engineer Committee (EEC) who aim to ensure that tomorrow's engineering leaders have access to knowledge owned by the current generation of engineers, and that that knowledge is passed on, in part, through DesignCon today.

Sierra Catelani, Test Engineer, ChargePoint
Hansel Dsilva, Signal Integrity Engineer, Achronix Semiconductor
Cathy George, System Engineer, Continental Automotive
Deepak Pai Hosadurga, RF Defense Engineer, Amazon Lab126
Abishek Manian, Analog Design Engineer, Texas Instruments
Scott Neally, Signal Integrity Engineer, Graphcore
Jinsung Youn, Research Scientist, Large-Scale Integrated Photonics, Hewlett Packard Labs
Tim Wang Lee, Signal Integrity Application Scientist, Keysight Technologies
Licheng (Joshua) Wu, Hardware Systems Engineer, NXP Semiconductors

DRIVE WORLD+ESC ADVISORY BOARD

We would like to thank the Drive World+ESC 2021 Advisory Board for their contributions as reviewers of all call-for-speaker submissions to develop a conference of the highest quality and industry relevance.

Mike Anderson, Embedded Systems Architect, The Aerospace Corporation
Daniel Beeker, Senior Principal Engineer, NXP Semiconductors
Jacob Beningo, President, Beningo Embedded Group
Chuck Brokish, Director of Transportation Business Development, Green Hills Software
Lindsay Craig, Entrepreneur/Engineer/Educator, QuestBotics
John Edwards, DSP and Embedded Systems Consultant, Numerix-DSP
Charles Fulks, Senior Engineer, Intuitive Research and Technology
Dwight Howard, Consultant
Eli Hughes, Co-Founder, Tzero
Randy Leberknight, Senior Firmware Engineer, Embedded Systems Consulting
Charles Lord, President, Blue Ridge Advanced Design and Automation
Phil Magney, Founder & President, VSI Labs
Gunnar Newquist, Product Manager, Hamilton Robotics
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Shawn Prestridge, US FAE Team Leader, IAR Systems
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August 18

Room 210F

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Advancing beyond

DESIGNCON® 2021
WHERE THE CHIP MEETS THE BOARD

GENERAL INFORMATION

LOCATION & DATES
DesignCon will take place August 16 -18, 2021, at the San Jose McEnery Convention Center in San Jose, CA. DesignCon welcomes its partner conference Drive World + ESC (Embedded Systems Conference) to the convention center in 2021.

CONFERENCE HOURS
Monday, August 16, 2021: 8:00 am – 6:00 pm
Tuesday, August 17, 2021: 8:00 am – 5:30 pm
Wednesday, August 18, 2021: 8:00 am – 5:30 pm

EXHIBIT HOURS
Tuesday, August 17, 2021: 11:00 am – 6:00 pm
Wednesday, August 18, 2021: 11:00 am – 6:00 pm

HEALTH & SAFETY
Health and safety are a top priority at this event. Visit DesignCon.com for up-to-date health and safety information and check the event app for any needed communications during the event.

REGISTRATION
All badges will be digital in 2021 and will be sent ahead of the event via email from DesignCon. Attendees, speakers, media, and exhibitors who need assistance with digital badging or who do not have a smartphone device that supports this feature can visit the event's registration area, located in room 220B. Please present a photo ID for assistance.

CHARGING STATIONS
Charging stations can be found at four locations throughout the event – the left and right sides of the expo floor, near Market Terrace and in the keynote hallway outside of the Grand Ballroom.

Sponsored by: MOUSER ELECTRONICS

WELCOME RECEPTION
Enjoy complimentary cocktails, picnic-themed foods, lawn games, and more at DesignCon's annual Welcome Reception, this year themed as a Family Reunion for engineers. Open to all pass types.

Sponsored by: samtec

CONCESSIONS
Concessions are available at the back of Exhibit Hall 1 at the San Jose McEnery Convention Center. The Convention Center is a cashless venue, only accepting credit cards or e-payment at concession stands.

CONFERENCE BREAKS
Conference breaks will be provided during conference break times for paid conference passholders, event committee members and speakers. The breaks will be located on the Market Terrace near the 210 and 211 session rooms.

Sponsored by: Tektronix® LEONI MathWorks®

CONFERENCE BREAKFAST
Complimentary breakfast is available on Monday, August 16 from 7:00 - 8:00 am in room 230A for all paid conference attendees, event committee members and speakers.

Sponsored by: MathWorks®

The program is subject to change without notice. Informa Markets reserves the right to alter venue, speakers, content, and/or other offerings.

THE TECHNICAL RENAISSANCE IS...

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Samtec is prepared for the technical renaissance with innovative Silicon-to-Silicon solutions that exceed standard connectivity demands.

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BOOTH 907

GENERAL INFORMATION

CONFERENCE NETWORKING LUNCH

Complimentary lunches are available daily for conference attendees, event committee members, and speakers.
Monday, August 16: Room 230A
Tuesday, August 17: Expo Hall 1
Wednesday, August 18: Expo Hall 1

Tuesday Sponsor: MathWorks®

CHIPHEAD THEATER

Check out the specialty programming in the Chiphead Theater featuring panels, training, and more right on the expo floor.

Sponsored by: KEYSIGHT TECHNOLOGIES

CAREER ZONE

The Career Zone is a designated area with targeted sessions to help you advance your career. Located on the expo floor, the full schedule can be found in the main agenda. Head shots will be provided on a first come first served basis. Sign up for 1:1 salary negotiation training at the Career Zone, beginning at expo open.

Sponsored by: SANMINA®

DIGITAL ZONE

Catch live interviews recorded with engineering thought leaders right on the expo floor in this new DesignCon feature.

Sponsored by: Rambus cadence®

PRODUCT SHOWCASE

See live, interactive demos at exhibitor booths as companies give you a first-hand look at their latest products and features. Demo schedule can be found in the main agenda.

BOOTH BAR CRAWL

Wind down at daily meet-and-greets around the expo floor, from 5:00 PM – 6:00 PM, Tuesday and Wednesday. Come for the conversation, stay for the bites and beverages.

Sponsored by: Rosenberger CARLISLE INTERCONNECT TECHNOLOGIES Amphenol ACE ACCURATE CIRCUIT ENGINEERING

PRESENTATION DOWNLOAD

Use the QR code below to download select speaker presentations. Note: Some presentations are available only for paid conference attendees. Login information will be emailed to paid conference attendees ahead of the event.

Tektronix®

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GENERAL INFORMATION

APP
This event utilizes a smartphone app to convey any event changes, as well as provide information on the event such as session details, venue maps, and hours. Use the QR code below to download the free event app.

EVALUATIONS
We value attendee feedback when planning the conference. Conference attendees can evaluate sessions using the below QR code.

INFORMATION DESK
An information desk is available in the event's registration area in room 220BC. Stop by if you have any questions on the event or need to speak to a member of event management.

INTERNET ACCESS
Wireless internet access is available throughout the building. Use the network Wickedly Fast WIFI – no password is required.

LOST & FOUND
Lost and found is located at event registration in room 220BC.

PUBLIC TRANSPORTATION & PARKING
Information on public transportation and the event's discounted parking rates can be found on DesignCon.com's Plan Travel tab.

MINORS
For safety, insurance, and security reasons, no one under the age of 18 is permitted in the expo halls or conference meeting rooms at the event. No childcare services are available onsite.

MEDIA CENTER
Located on the lower level of the San Jose McEnery Convention Center in room 113, the Media Center is open to registered exhibitors and their representatives, as well as members of the press and analysts. You must have a media badge for access. If you would like to set up any meetings please reach out to: pr.ime@informa.com.

SPEAKER CENTER
Located on the lower level of the San Jose McEnery Convention Center in room 114, the Speaker Center is open to registered speakers, as well as members of the DesignCon, Drive World, and ESC planning committees. You must have a speaker badge or be a current committee member for access.

INSTANT INSIGHTS MEETS IN-DEPTH INFORMATION

Attend the full-day seminar series

Tuesday, August 17th

8am-5pm in LL20 CD

VISIT BOOTH #607

INTRODUCING THE R&S®RTO6 OSCILLOSCOPE SERIES

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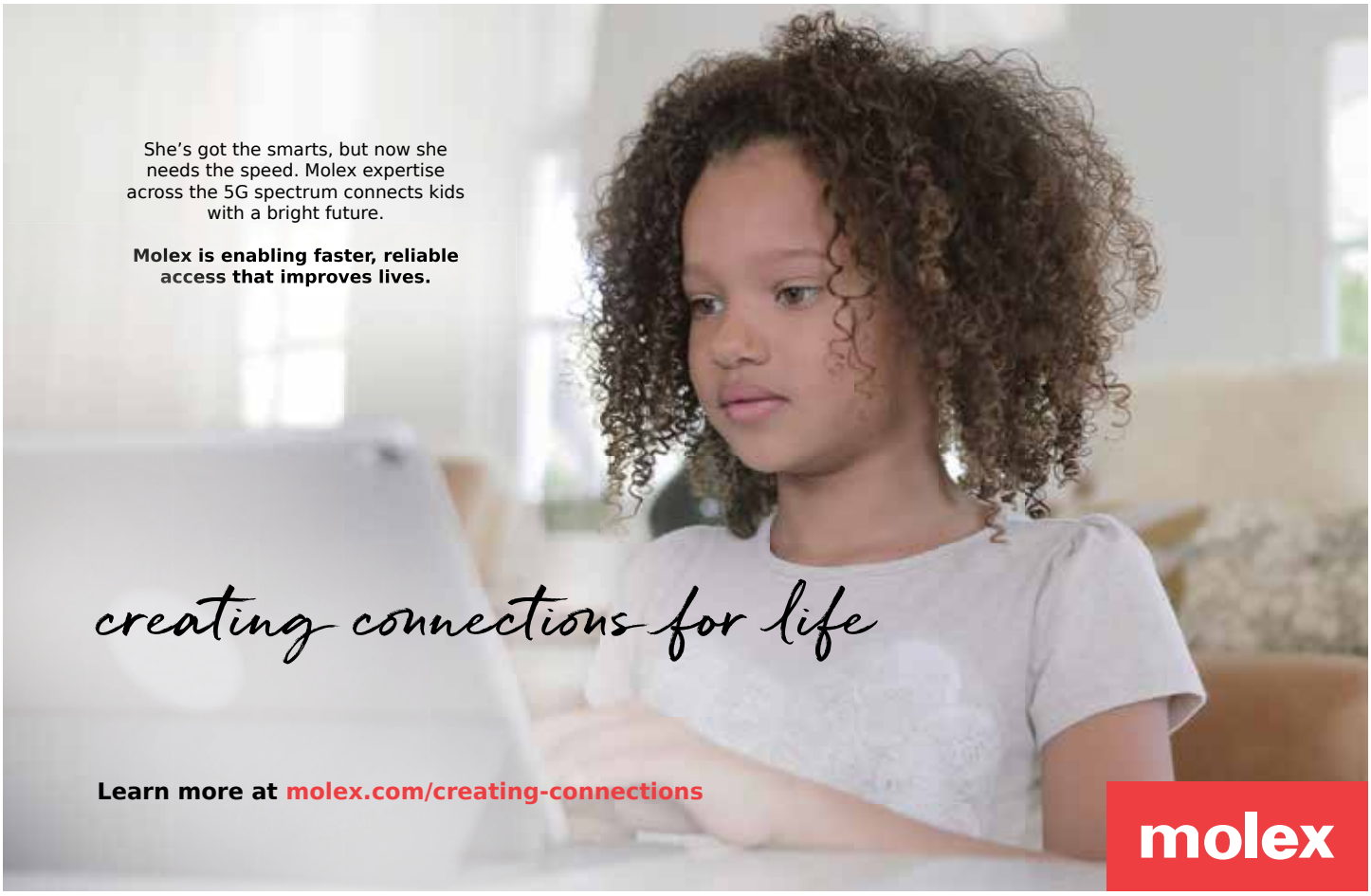


DesignCon® 2021

WHERE THE CHIP MEETS THE BOARD

KEYNOTES Open to All Attendees

Mike Fitton
VP, Data Platforms Group & GM,
Network Business Division at Intel

Beyond 5G: The Need for End-to-End Programmability

Monday, August 16
11:00 – 11:45 am
Grand Ballroom – 220A

5G has tremendous potential to enable revolutionary services, and 6G will see the convergence of compute and communication, all of which will stress our ability to deliver increasing performance within constrained power envelopes. This keynote will explore how these demands will drive the dual requirements of scalability and programmability.

Mark Wehde
Chair, Division of Engineering
Mayo Clinic

The Future of Healthcare is at the Edge

Tuesday, August 17
10:20 – 11:00 am
Grand Ballroom – 220A

The recent pandemic accelerated the transition from traditional hospital-centric medical care systems to a more virtual care—only made possible with advances in computational power, communications, and data storage. Conventional wisdom implies that the cloud is the future of healthcare, but the future of medical device innovation is really at the edge.

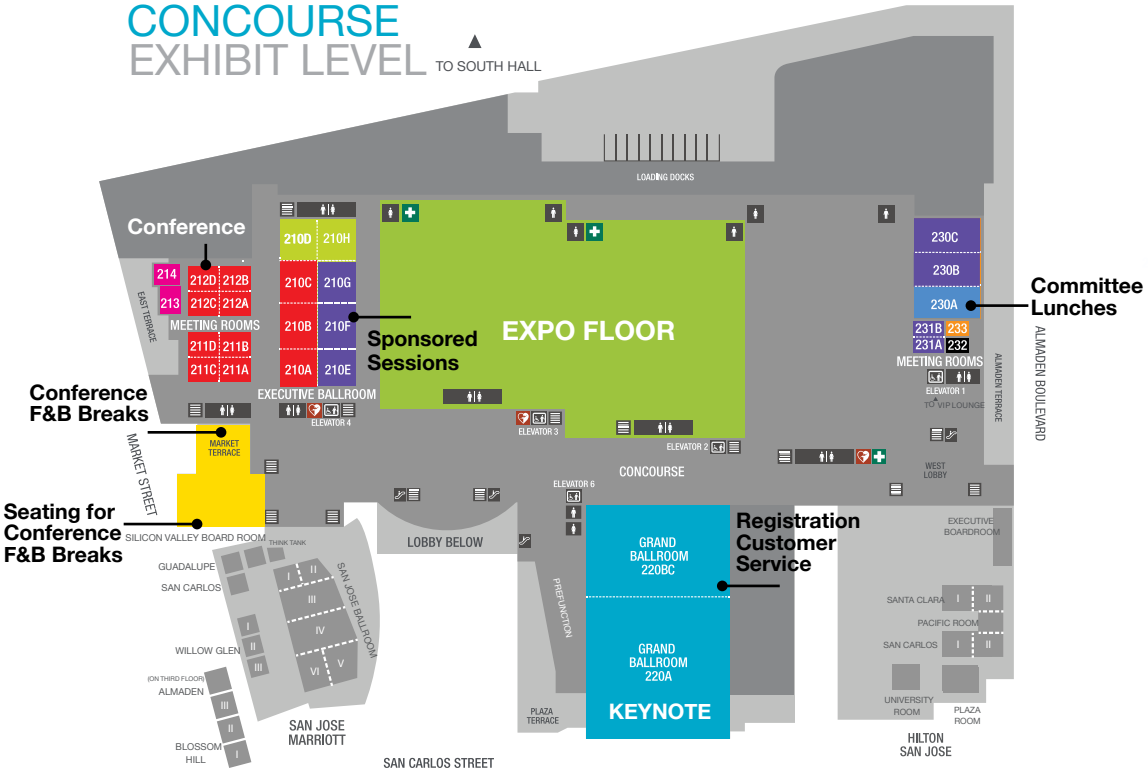
Indu Vijayan
Director of Product Management
for ADAS Solutions, AEye

Autonomous Vehicle Technology: Sensing What Matters

Wednesday, August 18
10:00 – 10:45 am
Grand Ballroom – 220A

What is the current market for autonomous vehicles, what are the growth drivers, and how does the industry solve the most challenging edge cases inhibiting broader rollouts? With a real-time, interactive driving demo, this keynote shows how AI-driven sensing is helping vehicles see smarter, respond faster, and accelerate adoption of autonomous features.

CONFERENCE MAP



SESSIONS – MONDAY, AUGUST 16

7:00 AM – 5:00 PM

Registration Open — Grand Ballroom 220BC

7:00 AM – 8:00 AM

Conference Breakfast
All-Access Pass, Boot Camp Pass, Drive World+ESC Pass, 2-Day Pass, Speakers, TPC, Media — Meeting Room 230A
Sponsored by: MathWorks

8:00 AM – 4:15 PM

Boot Camp — PI Ecosystem Simulation & Measurement: VRM + PDN + Digital Load
Access Pass, Boot Camp Pass — Meeting Room 211CD

Boot Camp — IBIS-AMI Model Creation
All-Access Pass, Boot Camp Pass — Meeting Room 211AB

8:00 AM – 10:30 PM

Tutorial — What is FEC & How Do I Use It?
All-Access Pass — Exec Ballroom 210A

Tutorial — Feeding the Beast: Consumption-based PCB Design
All-Access Pass — Exec Ballroom 210B

Tutorial — Powering the Connected Vehicle: A Focus on Energy Efficiency
All-Access Pass, Drive World+ESC Pass — Meeting Room 212C

Tutorial — Writing Reliable Multicore Code
All-Access Pass, Drive World+ESC Pass — Meeting Room 212D

11:00 AM – 11:45 AM

Keynote — Beyond 5G: The Need for End-to-End Programmability
Open to All — Grand Ballroom 220A

11:45 AM – 1:45 PM

Conference Networking Lunch
All-Access Pass, Boot Camps, Speakers, TPC — Meeting Room 230A

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App at m.designcon.com

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling & Validation Solutions
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement, Simulation & Improving Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

A. Drive World — Security & Safety
B. Drive World — Sensing Technologies
C. Drive World — Autonomous & ADAS
D. Drive World — Connectivity & Infotainment
E. ESC — Embedded Hardware Design & Verification
F. ESC — Embedded Software Design & Verification
G. ESC — IoT & Connected Devices
H. ESC — Advanced Technologies

- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- Career Zone
- General Event
- Special Event
- Sponsored Sessions

SESSIONS – MONDAY, AUGUST 16

1:45 PM – 4:15 PM

(4) Tutorial — PCB Design Principles for Implementing High Density Semiconductor Package Technology, WLP, PLP, 2D, 2.5D & 3D
All-Access Pass — Exec Ballroom 210C

(8) Tutorial — Design & Verification for High-Speed I/Os at 10 to 112 Gbps & beyond with Jitter, Signal Integrity & Power Optimized
All-Access Pass — Exec Ballroom 210A

(11) Tutorial — Radiated Emissions: Design for Compliance, Debugging & Pre-Compliance Testing
All-Access Pass — Exec Ballroom 210B

(B) Tutorial — The Building Blocks of Automated Vehicles
All-Access Pass, Drive World+ESC Pass — Meeting Room 212C

(E) Tutorial — Effective PCB Design: Techniques to Improve Performance
All-Access Pass, Drive World+ESC Pass — Meeting Room 212D

4:45 PM – 6:00 PM

(7) Panel — PCIe 6.0: New Challenges & New Tests for an Old Standard
Open to All — Exec Ballroom 210A

(8) (7) Panel — The Case of the Closing Eyes: Testing for 400G
Open to All — Meeting Room 211CD

6:00 PM – 8:00 PM

(★) DesignCon Family Reunion Welcome Reception — Sponsored by Samtec
Open to all DesignCon and Drive World+ESC Attendees, Exhibitors, Speakers, TPC, Media.
Badges Required for Entry. — Outdoor Plaza at the Idea Tree
Sponsored by: samtec

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App at m.designcon.com

- (1) Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
- (2) Chip I/O & Power Modeling & Validation Solutions
- (3) Integrating Photonics & Wireless in Electrical Design
- (4) Advances in Materials & Processing for PCBs, Modules & Packages
- (5) Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
- (6) System Co-Design: Modeling, Simulation & Measurement Validation
- (7) Optimizing High-Speed Link Design
- (8) Measurement, Simulation & Improving Jitter, Noise & BER
- (9) High-Speed Signal Processing, Equalization & Coding/FEC
- (10) Power Integrity in Power Distribution Networks
- (11) Electromagnetic Compatibility & Interference
- (12) Applying Test & Measurement Methodology
- (13) Modeling & Analysis of Interconnects
- (14) Machine Learning for Microelectronics, Signaling & System Design
- (A) Drive World — Security & Safety
- (B) Drive World — Sensing Technologies
- (C) Drive World — Autonomous & ADAS
- (D) Drive World — Connectivity & Infotainment
- (E) ESC — Embedded Hardware Design & Verification
- (F) ESC — Embedded Software Design & Verification
- (G) ESC — IoT & Connected Devices
- (H) ESC — Advanced Technologies
- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- Career Zone
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SESSIONS – TUESDAY, AUGUST 17

7:00 AM– 6:00 PM

Registration Open — Grand Ballroom 220BC

8:00 AM – 8:40 AM

Enabling an XSR Channel for an Optical Co-packaged Ethernet Switch (3, 6)
All-Access Pass, 2-Day Pass — Meeting Room 212AB

The Impact of Emerging Ultra-thin Film PCB Laminates Technology on PDN Architecture & Power Noise Reduction Strategies (4, 10)
All-Access Pass, 2-Day Pass — Meeting Room 211AB

Validation Techniques for DDR5 RDIMM Power Management Systems (5, 10)
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

In Situ LPDDR4 Interposer Created on HDI PCB for Debugging & Testability (6, 12)
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Specification-based IBIS-AMI Model PCIe 5.0 32GT/s (7, 2)
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

8:00 AM – 8:40 AM

A Generalized PSIJ Sensitivity Analysis Method Based on PSRR Response (8)
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Transitioning from R&D Software to Safe Autonomous Systems (A)
All-Access Pass, 2-Day Pass,
Drive World+ESC Pass — Meeting Room 212C

In-Situ De-embedding
Open to All — Exec Ballroom 210F

8:30 AM – 9:10 AM

Advanced Testing Challenges at 32GBaud PAM4 with PCIe 6.0
Open to All — Exec Ballroom 210E

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1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
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4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement, Simulation & Improving Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
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SESSIONS – TUESDAY, AUGUST 17

9:00 AM – 9:40 AM

Receiver Design Drives Optical Transmitter Test in the PAM4 Era
(3) (12)
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

Fiber Weave Intra-pair Skew Analysis & Mitigation on 32-Gbps NRZ & 64-Gbps PAM4
(7)
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Capacitor Placement Strategies for Optimum Power Integrity
(10) (11)
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Neural Language Model Enables Extremely Fast & Robust Routing on Interposer
(14)
All-Access Pass, 2-Day Pass — Meeting Room 211AB

Getting Started with Multicore Microcontroller Applications
(H)
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

Emerging Compute Architectures for the Evolving Data Center
Open to All — Exec Ballroom 210G

9:00 AM – 9:40 AM

Analysis of Electro-static Discharge to Through-silicon Via
(11)
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Developing Good Test Fixtures for De-embedding of S-Parameters
Open to All — Exec Ballroom 210F

Wireless Memory Test: A Breakthrough Solution for Highly Reliable HBM
(1) (3)
All-Access Pass, 2-Day Pass — Exec Ballroom 212AB

9:20 AM – 10:05 AM

Next Gen Development in Type-C Ecosystem
Open to All — Exec Ballroom 210E

9:50 AM – 10:20 AM

DesignCon Awards Presentations
Open to All — Grand Ballroom 220A

10:20 AM – 11:00 AM

Keynote — The Future of Healthcare is at the Edge
Open to All — Grand Ballroom 220A

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SESSIONS – TUESDAY, AUGUST 17

11:00 AM – 11:50 AM

Mastering Phase Noise/Jitter Measurements
Open to All — Exec Ballroom 210F

11:00 AM – 6:00 PM

Expo Hall Open
Open to All — Expo Hall

11:10 AM – 11:50 AM

COM based IBIS-AMI for 106/112Gbps System Compliance
2
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

A Case Study in the Development of a 112Gbps-PAM4 Silicon & Connector Test Platform
6 7
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

BER Optimization Through Noise-shaping & Precoding for 112-G SerDes Applications
7
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Predicting Emissions Properties
11
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Evaluating Fixture Removal Techniques for Sensitivities & Uncertainties
12 13
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

11:10 AM – 11:50 AM

Crosstalk & Return Loss Budget Trade-Offs Among Different Sections in the SerDes Channel
13 7
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Power Integrity Principals for nm-CMOS Devices
10 1
All-Access Pass, 2-Day Pass — Exec Ballroom 211AB

Debugging V2X Systems for Safety & Security
A
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

Selecting the Right High-Performance Memory Solution
Open to All — Exec Ballroom 210G

11:15 AM – 11:55 AM

Bench Top Troubleshooting the Top Three EMC Issues: Radiated Emissions, Radiated Immunity & ESD
Open to All — Chiphead Theater (Booth 122)

Physical Layer Validation Challenges of Characterizing 100 Gbps/lane Designs
Open to All — Exec Ballroom 210E

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SESSIONS – TUESDAY, AUGUST 17

11:30 AM – 11:45 AM

Product Showcase: Samtec
Open to All — Booth 907

12:05 PM – 12:45 PM

Solving Your Forward Error Correction Problems
Open to All — Exec Ballroom 210E

12:00 PM – 12:15 PM

Product Showcase: Xpeedic Technology, Inc.
Open to All — Booth 913

12:00 PM – 1:30 PM

Career Zone — Women & Minorities in STEM
Open to All — Booth 1025

12:10 PM – 12:50 PM

Designing 224-G High Performance FPGA Package & Board with Confidence
1, 13
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Plated-through-hole Via Design Specifications for 112-G Serial Links
4, 7
All-Access Pass, 2-Day Pass — Meeting Room 212AB

12:10 PM – 12:50 PM

Enabling Secure SoC Design by Fast Power-noise & EM Side-channel Emission Analysis
6, 10
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Effects of Via Configurations on End-to-End System-Level Performance for PCIe Gen5 Modular Solutions
7, 13
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Cost-effective Power Integrity Methodology for Integrating Next-generation High-speed IPs
10
All-Access Pass, 2-Day Pass — Meeting Room 211CD

System Level Impact to 100-Gb/s Electrical Signaling Due to Common to Differential Mode Conversion
13, 6
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

Implementing PCI Express and CXL Interface Solutions
Open to All — Exec Ballroom 210G

Accurately Measuring Data Dependent Jitter on High Bitrate Signals
Open to All — Exec Ballroom 210F

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SESSIONS – TUESDAY, AUGUST 17

12:15 PM – 12:55 PM

Armour-Plating Your C/C++ Code
Open to All — Chiphead Theater (Booth 122)

12:30 PM – 2:30 PM

Conference Networking Lunch
All-Access Pass, Boot Camps, Speakers, TP — Expo Hall
Sponsored by: MathWorks

1:15 PM – 1:55 PM

Survive & Thrive in the Coming Semiconductor "Capacity War"
Open to All — Chiphead Theater (Booth 122)

1:45 PM – 3:15 PM

Career Zone — Emerging Engineers Networking
Open to All — Career Zone (Booth 1025)

2:00 PM – 2:15 PM

Product Showcase: Rohde & Schwarz USA Inc.
Open to All — Booth 607

2:00 PM – 6:00 PM

Career Zone — 1:1 Salary Negotiation Advice
Open to All — Career Zone (Booth 1025)

2:00 PM – 2:40 PM

Holistic Power Supply Induced Jitter Accumulation Response Surface Modeling for Chiplet Interconnect System
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Hidden Secrets of IBIS Sampling Specifications
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Multimode System Design for PIC (Photonic Integrated Circuit) Integration
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

112G+ Crosstalk Simulation of Differential Lines Based on MOP Model
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Next Generation 224-Gbps Highest-Speed Electrical I/O & Link Systems
All-Access Pass, 2-Day Pass — Meeting Room 211AB

USB4 Cable & Connector Design for Client Systems
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Increasing Code Security by implementing MISRA C & SEI CERT C
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

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SESSIONS – TUESDAY, AUGUST 17

2:00 PM – 2:40 PM

High-Speed Digital Test Fundamentals
Open to All — Exec Ballroom 210F

What's Next for High-Bandwidth Memory?
Open to All — Exec Ballroom 210G

2:15 PM – 2:55 PM

The Modernization of Test & Measurement
Open to All — Chiphead Theater (Booth 122)

3:00 PM – 3:15 PM

Product Showcase: Keysight Technologies
Open to All — Booth 807

3:00 PM – 3:40 PM

Highly Integrated Silicon Photonics Technology Beyond 800Gbps
3
All-Access Pass, 2-Day Pass — Meeting Room 212AB

From Simulation to Production: An In-Depth Look at Designing and Productizing GDDR6x, the World's First PAM-4 Memory Interface
5 6
All-Access Pass, 2-Day Pass — Meeting Room 211AB

Electrical Optimization for Small Form Factor Systems
6 13
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

3:00 PM – 3:40 PM

Design Case Study & Experimental Validation for a 100 Gb/s Per Lane C2M Link Using Channel Operating Margin
7 6
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Extreme Measurement Challenges
12
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Windowing & Risetime
13 8
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

Adaptive MAP & SPaT Messaging Techniques for Autonomous Vehicles: A Smart Cities Case Study
B
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

Automated Failure Analysis of Remote Edge Devices at Scale
F
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

Power Integrity Measurement Fundamentals
Open to All — Exec Ballroom 210F

Integrated MIPI IP Solutions for Next-Generation Displays
Open to All — Exec Ballroom 210G

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SESSIONS – TUESDAY, AUGUST 17

3:15 PM – 3:55 PM

Panel — Building an Autonomous Test Vehicle
Open to All — Chiphead Theater (Booth 122)

3:30 PM – 4:30 PM

Career Zone — How to Start a Start-Up Discussion
Open to All — Career Zone (Booth 1025)

4:00 PM – 5:15 PM

Panel — Interoperable Common Electrical Interfaces (CEI) & Channel Standards Update: An OIF Perspective
Open to All — Meeting Room 211AB

Panel — Avoiding Disaster: Planning for Laminate Electrical Properties as a Function of Temperature
Open to All — Meeting Room 212AB

4:00 PM – 4:40 PM

Automotive SERDES technology and measurements from1000BASE-T1 to 10GBASE-T1
Open to All — Exec Ballroom 210F

2.5D/3D Packaging Solutions for AI and HPC
Open to All — Exec Ballroom 210G

4:15 PM – 4:55 PM

Electromagnetic Fields for Normal Folks
Open to All — Chiphead Theater (Booth 122)

4:30 PM – 6:00 PM

Career Zone — Open Networking
Open to All — Career Zone (Booth 1025)

5:00 PM – 6:00 PM

Booth Bar Crawl
Open to All — Beer Halls at Front & Rear of Expo Floor
Sponsored by: Rosenberger, CARLISLE INTERCONNECT TECHNOLOGIES

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SESSIONS – WEDNESDAY, AUGUST 18

7:00 AM — 6:00 PM

Registration Open — Grand Ballroom 220BC

8:00 AM — 8:40 AM

Reflection Removal for High-speed Signal Link & Mid-bus Probing
1, 8
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

LPDDR5 (6.4 Gbps & Beyond) 1-tap & Multi-tap DFE Optimal Weights for Signal Integrity
6, 5
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

Proposal for Automated E-O-E IBIS-AMI Modeling
7, 3
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Alternate Power Integrity Analysis Methodology: PCBs, FPGAs, ASICs & MCMs
10, 1
All-Access Pass, 2-Day Pass — Meeting Room 211AB

Two Novel Skew Compensation Techniques for Reducing Mode Conversion
11, 7
All-Access Pass, 2-Day Pass — Meeting Room 212AB

8:00 AM — 8:40 AM

Machine Learning Based Backchannel Mechanism for Expert-free High-speed Link Equalization Tuning
14, 7
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Architecting a Secure Central Vehicle Gateway: Using OPEN Source Software
D
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

Embedded Safety & Security: Shift Left & Design It Right
E
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

8:30 AM — 9:10 AM

Quick Guide to Recalibrate Your Signal Integrity Intuition for Memory Interfaces
Open to All — Exec Ballroom 210E

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SESSIONS – WEDNESDAY, AUGUST 18

9:00 AM — 9:40 AM

(1) Voltage-dependency Effect of Through-silicon Vias on the Power Distribution Network
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

(3) (7) Comprehensive End-to-end Link Modeling & Simulation with Silicon Photonics & SerDes Transceivers
All-Access Pass, 2-Day Pass — Meeting Room 211CD

(4) Air as a Primary Dielectric to Minimize Losses
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

(9) (7) Salz SNR & Shannon Limit Study for the Next Speed Node Beyond 112Gbps (& up to 224Gbps)
All-Access Pass, 2-Day Pass — Meeting Room 211AB

(11) (10) Impact of Power Plane Termination on System Noise
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

(8) (12) (9) Considerations for Reference Equalizer Optimization at 112Gbps
All-Access Pass, 2-Day Pass — Meeting Room 212AB

9:00 AM — 9:40 AM

(D) PCI Express Technology: Accelerating Automotive Connectivity, from Infotainment to ADAS
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

(E) DevOps for Hardware Junkies: Closing the Gap with Automated Infrastructure
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

Importance of Sequential Peeling Extraction and De-embedding When Designing PCBs
Open to All — Exec Ballroom 210F

9:20 AM — 10:05 AM

Ramping Up on the Latest Skills for Power Integrity Design/Debug
Open to All — Exec Ballroom 210E

10:00 AM — 10:45 AM

(★) Keynote — Autonomous Vehicle Technology: Sensing What Matters
Open to All — Grand Ballroom 220A

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SESSIONS – WEDNESDAY, AUGUST 18

10:15 AM — 11:15 AM

Open House for PCIe 5.0 RX LEQ Test Live demo (Walk in at any time!)
Open to All — Exec Ballroom 210F

11:00 AM — 6:00 PM

Expo Hall Open
Open to All — Expo Hall

11:10 AM — 11:50 AM

An Innovative Power Decoupling Solution using Integrated Stack Capacitor (ISC) for High-Performance Computing Systems
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Design of a Hybrid Equalizer for 12.8-Gb/s High Bandwidth Memory Gen. 4
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

System Design for 112G: Device Characteristics, Channel Details & Expected System Performance
All-Access Pass, 2-Day Pass — Meeting Room 211AB

11:10 AM — 11:50 AM

IP/PHY Solutions & Rigorous Characterization are Critical for Successful USB4/Thunderbolt 4 Implementations
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Innovative Designs for Optimizing 112G+ BGA Fan-out And Connector Footprint Crosstalk
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Model-based Digital Twin for Anomaly Detection of On-Chip Transient Thermal Response
All-Access Pass, 2-Day Pass — Meeting Room 211CD

5G's Future Impact on CV2X
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

PCB Design Techniques to Improve ESD Robustness
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

PAM4 BER and JTOL Test Solution for PCIe® 6.0and Beyond
Open to All — Exec Ballroom 210F

TRACKS AND LEGEND

To See Speakers for Each Session – Download the DesignCon Event App at m.designcon.com

1. Signal & Power Integrity for Single-Multi Die, Interposer & Packaging
2. Chip I/O & Power Modeling & Validation Solutions
3. Integrating Photonics & Wireless in Electrical Design
4. Advances in Materials & Processing for PCBs, Modules & Packages
5. Advanced I/O Interface Design for Memory & 2.5D/3D/SiP Integrations
6. System Co-Design: Modeling, Simulation & Measurement Validation
7. Optimizing High-Speed Link Design
8. Measurement, Simulation & Improving Jitter, Noise & BER
9. High-Speed Signal Processing, Equalization & Coding/FEC
10. Power Integrity in Power Distribution Networks
11. Electromagnetic Compatibility & Interference
12. Applying Test & Measurement Methodology
13. Modeling & Analysis of Interconnects
14. Machine Learning for Microelectronics, Signaling & System Design

A. Drive World — Security & Safety
B. Drive World — Sensing Technologies
C. Drive World — Autonomous & ADAS
D. Drive World — Connectivity & Infotainment
E. ESC — Embedded Hardware Design & Verification
F. ESC — Embedded Software Design & Verification
G. ESC — IoT & Connected Devices
H. ESC — Advanced Technologies

- Best Paper Awards Finalist
- Boot Camp
- Chiphead Theater Presentation
- Career Zone
- General Event
- Special Event
- Sponsored Sessions

SESSIONS – WEDNESDAY, AUGUST 18

11:15 AM — 11:55 AM

Next Generation Memory Solutions
Open to All — Exec Ballroom 210E

Live Hack: Exposing Common IoT Security Weaknesses
Open to All — Chiphead Theater (Booth 122)

12:00 PM — 12:45 PM

Live Demo of PAM4 BERT and JTOL, FEC and BurstError Analysis
Open to All — Exec Ballroom 210F

12:05 AM — 12:45 AM

Explore Why Testing Disaggregated 5G Elements in Isolation is Required to Ensure Proper O-RAN Fronthaul Conformance
Open to All — Exec Ballroom 210E

12:10 PM — 12:50 PM

The Path to 200-Gbps Serial Links
13 7
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Advanced Modeling for Novel High-performing Low-cost Copper Foils
4 13
All-Access Pass, 2-Day Pass — Meeting Room 211AB

Error Signature Generation from IBIS-AMI Link Simulations
9 8
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Capacitor Optimization in Power Distribution Networks Using Numerical Computation Techniques
10
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Analytical Prediction of EM Radiation from Stacked Trays in Data Centers
11 12
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Bridging the Organization Gap for EDA Machine Learning Data
14
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

TRACKS AND LEGEND

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SESSIONS – WEDNESDAY, AUGUST 18

12:10 PM — 12:50 PM

A Foundation for Autonomy: New Automotive Standards Accelerate Development of Autonomous Vehicles
All-Access Pass, 2-Day Pass, Drive World+ESC Pass
Meeting Room 212C

Internet of Insecure Things: Through the Eyes of a Hacker
All-Access Pass, 2-Day Pass, Drive World+ESC Pass
Meeting Room 212D

12:15PM — 12:55 PM

PC Board Design for Low EMI for Wireless & IoT
Open to All
Chiphead Theater (Booth 122)

12:30 PM — 1:45 PM

Career Zone — DesignCon 2022 Paper Topic Consultations
Open to All
Career Zone (Booth 1025)

12:30 PM — 2:30 PM

Conference Networking Lunch
All-Access Pass, Boot Camps, Speakers, TPC
Expo Hall

1:15 PM — 1:55 PM

Developing Edge Devices for Chronic Disease Management
Open to All
Chiphead Theater (Booth 122)

2:00 PM — 6:00 PM

Career Zone — Headshots & Networking Reception
Open to All
Career Zone (Booth 1025)

2:00 PM — 2:40 PM

A New Design Method of GDDR6 WCLK Using Reinforcement Learning for over 20Gbps
All-Access Pass, 2-Day Pass
Exec Ballroom 210B

A New Approach to IBIS-AMI Modeling of Single-Ended Memory Interfaces
All-Access Pass, 2-Day Pass
Meeting Room 211AB

Signal Integrity Analysis in Immersion Liquid Cooling
All-Access Pass, 2-Day Pass
Meeting Room 212AB

SNDR Analysis & Its Impacts on Link Performance
All-Access Pass, 2-Day Pass
Meeting Room 211CD

Divide & Conquer Approach to Radio Frequency Interference Simulation
All-Access Pass, 2-Day Pass
Exec Ballroom 210C

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SESSIONS – WEDNESDAY, AUGUST 18

2:00 PM — 2:40 PM

Effect of the Maximum Frequency & Frequency Resolution of S Parameters on Channel Simulation
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

Technical & Regulatory Incentives to Accelerate Level 4 Autonomous Driving
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

IoT Security Throughout the Entire Lifecycle
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212D

Automotive Test Solutions
Open to All — Exec Ballroom 210F

2:15 PM — 2:55 PM

Building Safe & Secure Systems Using OPEN Source
Open to All — Chiphead Theater (Booth 122)

3:00 PM — 3:40 PM

Optimizing BGA Ball Pattern for Signal Integrity
All-Access Pass, 2-Day Pass — Exec Ballroom 210A

End-to-end IBIS-AMI Modeling & Simulations of Electrical/Optical Links
All-Access Pass, 2-Day Pass — Meeting Room 211CD

Electronic-Photonic IC Co-Design with Signal/Power Integrity and Thermal Simulation for Silicon Photonics 3D IC
All-Access Pass, 2-Day Pass — Meeting Room 211AB

100G Chip-to-Module Interface Challenges & New Measurement Methodology
All-Access Pass, 2-Day Pass — Meeting Room 212AB

Machine Learning for TDECQ: Accelerating Transceiver Characterization & Verification
All-Access Pass, 2-Day Pass — Exec Ballroom 210C

Global Optimization of Wireline Transceivers for Minimum Post-FEC vs. Pre-FEC BER
All-Access Pass, 2-Day Pass — Exec Ballroom 210B

Enabling the Deployment of True Driverless Vehicles
All-Access Pass, 2-Day Pass, Drive World+ESC Pass — Meeting Room 212C

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SESSIONS – WEDNESDAY, AUGUST 18

3:00 PM — 3:40 PM

G IoT Endpoints Transformed by Intelligence
All-Access Pass, 2-Day Pass,
Drive World+ESC Pass
Meeting Room 212D

USB Type-C® Standard PHY testing. What's the same, and what's different?
Open to All
Exec Ballroom 210F

3:15 PM — 3:55 PM

Protecting Autonomous Vehicle Innovations: Key IP Strategies for the Present & Future
Open to All
Chiphead Theater (Booth 122)

4:00 PM — 5:15 PM

3 Panel — Getting Onboard (& Package) with Photonics: What'll It Take?
Open to All
Meeting Room 212AB

C Panel — Bringing AI to the Edge: Hardware & Software Enables Autonomous AI Ecosystem on the Edge
Open to All
Meeting Room 212C

4:00 PM — 5:00 PM

PCIe 5.0 Receiver LEQ Compliance Test
Open to All
Exec Ballroom 210F

5:00 PM — 6:00 PM

Booth Bar Crawl
Open to All
Beer Halls at Front & Rear of Expo Floor
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Drive
WORLD CONFERENCE & EXPO

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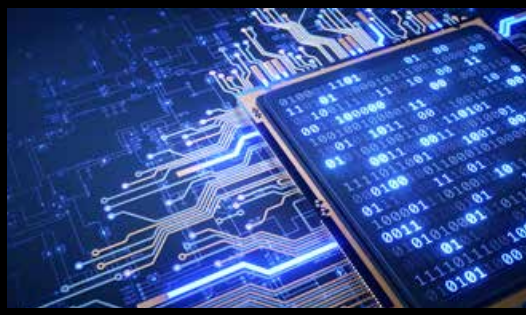
EMBEDDED SYSTEMS CONFERENCE

Drive World+Embedded Systems Conference (ESC)

August 16 -18, 2021 | San Jose McEnery Convention Center







In its second year, Drive World+ESC will return to Silicon Valley to bring together the brightest minds across automotive electronics, embedded systems, and IoT who shape the technology of tomorrow.

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EXHIBITOR LIST

Company	Booth
219 Design	516
Accurate Circuit Engineering	325
ACES	821
Advanced Test Equipment Rentals	825
AGC Multi Material, Inc.	719
AiSHi Capacitors	627
Amphenol	707
APCT	924
ARC Technologies, Inc.	316
ARTEK Inc.	428
Avishtech	521
Bellwether Electronic Corp	421
CarlisleIT	724
Co-Tech Development Corp.	335
Cvilux USA	625
Doosan Corporation Electro-Materials BG	507
DVT Solutions, LLC	831
Electro Rent Corporation	917
EMA Design Automation Inc.	414
Ept	415
eTopus Technology Inc	531
evissaP	216
Flexible Circuit Technologies Inc	219
Fotofab, LLC	218
Foxconn Interconnect Technology	315
Gigatest Labs	606
Granite River Labs	835

Company	Booth
Harwin	307
Huber+Suhner	930
Hyperlabs	410
Imagineering Inc.	417
Innosilicon	914
Insulated Wire Inc	433
Ironwood Electronics	418
Isola Group	925
ITEQ Corporation	425
Jess-Link Products Co. Ltd.	630
Junkosha Inc.	827
Kandou Bus S.A.	207
Keysight Technologies	807
KGS America Inc.	424
Langer EMV-Technik GmbH	214
Leeno Industrial Inc.	1013
Luxshare-ICT	615
Marki Microwave, Inc.	208
MPI Corporation	432
MultiLane Inc	931
Neoconix	434
Oak-Mitsui Technologies	815
Ohmega | Ticer Technologies	817
OMDIA	427
PacketMicro, Inc.	511
PalPilot International	306
Panasonic Industrial Devices Sales Company of America	728
PFC Flexible Circuits	435
Plastronics	635

Company	Booth
Polar Instruments	420
Printed Circuit Engineering Association	537
Rigol Technologies Usa	1007
Riva HQ	638
Rogers Corporation	319
Rohde & Schwarz USA, Inc.	607
Rosenberger North America	515
Royal Circuits	329
Samtec	907
Senko	333
Siglent Technologies Co., Ltd.	820
Silitronics	524
Socionext America Inc.	532
Somacis Inc.	634
Sonnet Software	318
Southwest Microwave	514
SRC Inc.	934
Sumitomo Electric Industries	311
Surface Mount Technology Association	636
SV Microwave	530
TDK - Lambda High Power Division	321
Technica, USA	406
Tempo Automation	217
US Conec, Ltd	535
Versatile Power	431
Victory Giant Technology	926
VSI Labs	407
Xpeedic Technology Inc.	913

EXHIBIT HALL FLOOR MAP

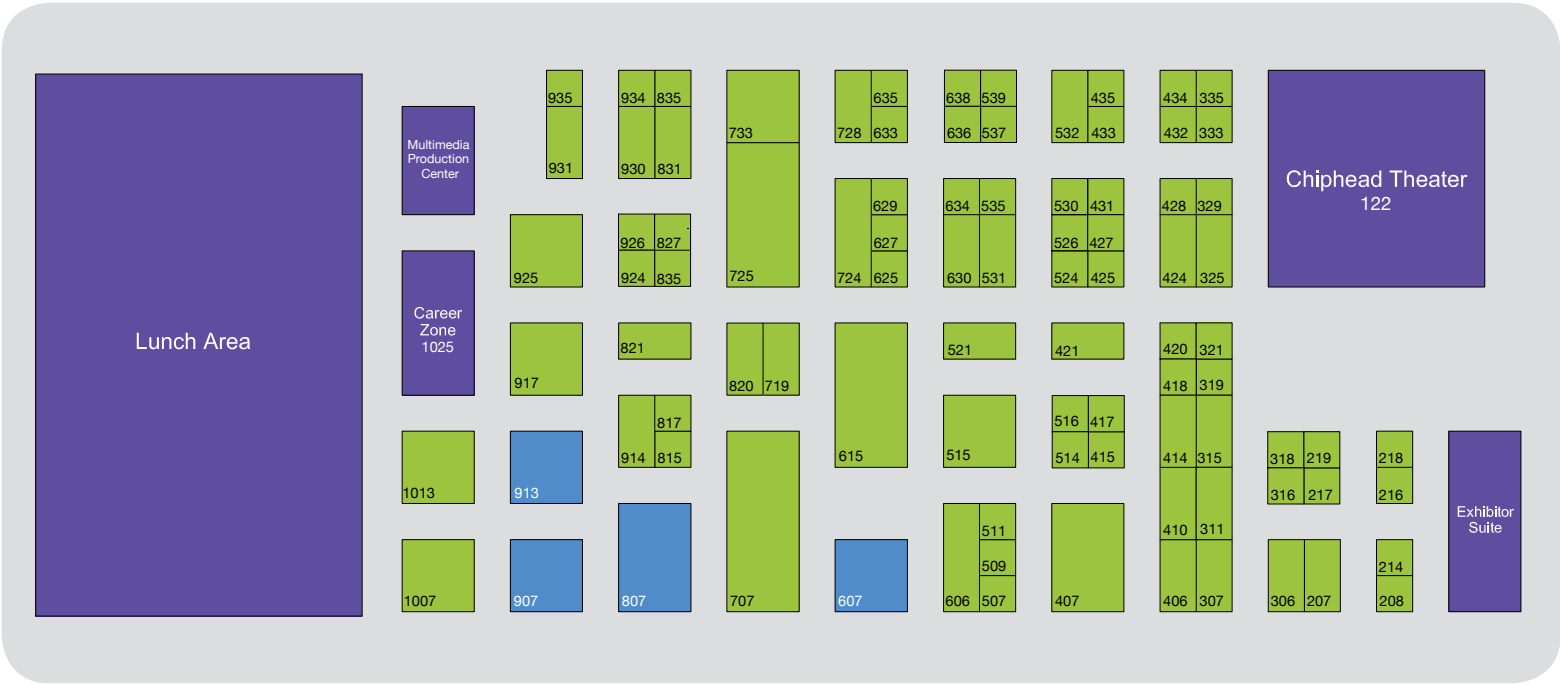

EXHIBIT HOURS:

AUGUST 17 – 18, 2021 / 11:00 AM - 6:00 PM

Tuesday Product Showcase Locations

DesignCon Event App
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We will be sharing and interacting with our followers during DesignCon, helping drive additional attention to you through DesignCon's followers.

Product Showcase

Don't miss this series of LIVE demos taking place on the DesignCon show floor.

TUESDAY, AUGUST 17, 2021

TIME	COMPANY	BOOTH
11:30 am	samtec	907
12:00 pm	XPEEDIC ACCELERATE YOUR IC DESIGN	913
2:00 pm	ROHDE&SCHWARZ Make ideas real	607
3:00 PM	KEYSIGHT TECHNOLOGIES	807

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CareerZone

Be sure to stop by the DesignCon Career Zone in the expo hall to gain advice on advancing your career and salary, get tips on presenting at technical conferences, network, connect 1:1, or receive a complimentary professional headshot.

WOMEN & MINORITIES IN STEM

Why are there so few women and members of minorities in STEM? This discussion and networking session will explore the challenges and opportunities for women and minorities in STEM fields.

August 17, 2021 | 12:00 – 1:30 pm

EMERGING ENGINEERS NETWORKING

Come meet your fellow leaders of tomorrow's innovations. At this session DesignCon welcomes engineers who are starting their professional journey or who have less than 10 years of experience. Grow your network and connect with like-minded peers and members of DesignCon's Emerging Engineer Committee at this networking session.

August 17, 2021 | 1:45 – 3:15 pm

HOW TO START A START-UP DISCUSSION

Silicon Valley is a hotbed for start-ups but not all thrive or even survive. Connect with entrepreneurs and organizations in the San Jose-area who have not only started a business but sustained and grown it.

August 17, 2021 | 3:30 – 4:30 pm

OPEN NETWORKING

Connect with others looking to advance their careers during this open networking session.

August 17, 2021 | 4:30 – 6:00 pm

1:1 SALARY NEGOTIATION ADVICE

Is it time to make a change to your salary? Experts from Riva will offer 1:1 advice on advancing your salary. These meetings are by appointment only and will fill quickly! Sign up at the DesignCon Career Zone starting at 11:00 am.

August 17, 2021 | 2:00 – 6:00 pm

DESIGNCON 2022 PAPER TOPIC CONSULTATIONS

Are you considering submitting a paper for DesignCon 2022 but unsure of the best topic, track, or makeup of the paper? Members of the DesignCon Technical Program Committee will be available to answer your paper submission questions and provide advice on best practices.

August 18, 2021 | 12:30 – 1:45 pm

HEADSHOTS & NETWORKING RECEPTION

Advance your LinkedIn profile and other professional efforts with a complimentary headshot from a Lunch Break Headshots professional photographer. And while you're at it, make sure to enjoy the DesignCon Booth Bar Crawl (5-6pm), offering refreshments while you network.

August 18, 2021 | 2:00 – 6:00 pm

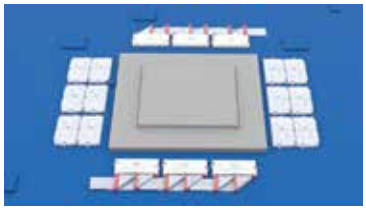
Amphenol

Amphenol will be presenting Innovative Product Demonstrations at booth #707

High Speed IO

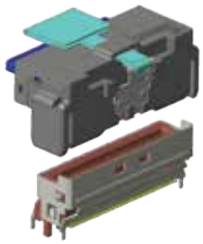
High Speed Backplane

OverPass™ Solutions



Mezzanine

Storage & Server IO



AssembleTech

Enabling the Electronics Revolution

DesignCon® 2021

WHERE THE CHIP MEETS THE BOARD

BOOTH BAR Crawls

Wind down at daily meet-and-greets at the front and back of the expo floor. Come for the conversation, stay for the bites and beverages.

TUESDAY, 5:00 – 6:00 PM

Rosenberger

CARLISLE INTERCONNECT TECHNOLOGIES

WEDNESDAY, 5:00 – 6:00 PM

Rosenberger

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PCEA Printed Circuit Engineering Association

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Signal Integrity Journal

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VSI Labs

Women in Autonomy

Health & Safety Are A Top Priority!

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Wear your mask while indoors

Avoid handshakes and wash your hands frequently

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Visit DesignCon.com for up-to-date information regarding health & safety.

Digital Badging At DesignCon 2021

How it Works

Expo floor, session room, and networking access has gone digital this year, which means quicker entry into the event. To save your digital credential, follow these simple steps:

- Watch for an email from DesignCon with your digital credential QR Code.
- Depending on your device, choose either the Apple Wallet or Google Pay.
- Load the digital credential to your wallet.

Then when you're onsite, just open the digital credential on your phone (like you would for a mobile boarding pass), have it scanned, and you're good to go!

No smart phone? No problem. Just visit the on-site registration area and print out your credentials.

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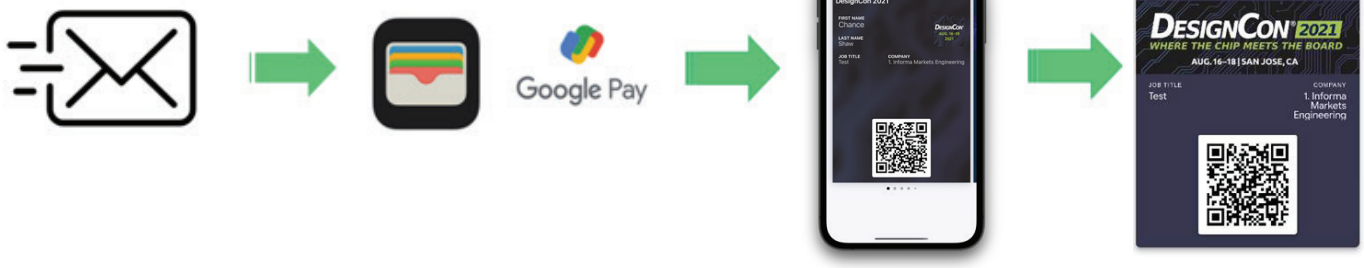
4. Open Badge



2021 Engineer of the Year

The winner will be selected based on his or her leadership, creativity, and out-of-the-box thinking brought to design/test of chips, boards, or systems, with particular attention paid to areas of signal and power integrity.

DesignCon 2020 Best Paper AWARD WINNER

Each year DesignCon recognizes outstanding contributions to the educational goals of the DesignCon program.

The **Best Paper Awards** serve to acknowledge the authors who receive them as leading practitioners in semiconductor and electronic design.

When: Tuesday, August 17, 2021, 9:50 – 10:20 am
Where: Grand Ballroom 220A

DesignCon® 2021

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JOIN the Conversation

- **POST** a photo of your favorite booth
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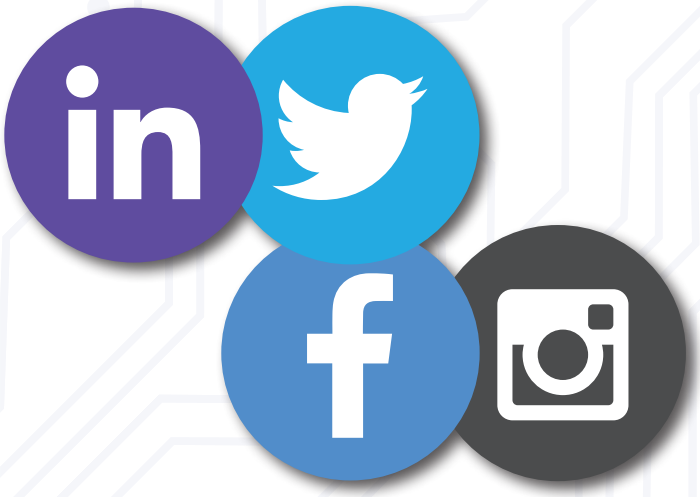
- **NETWORK** with fellow industry professionals



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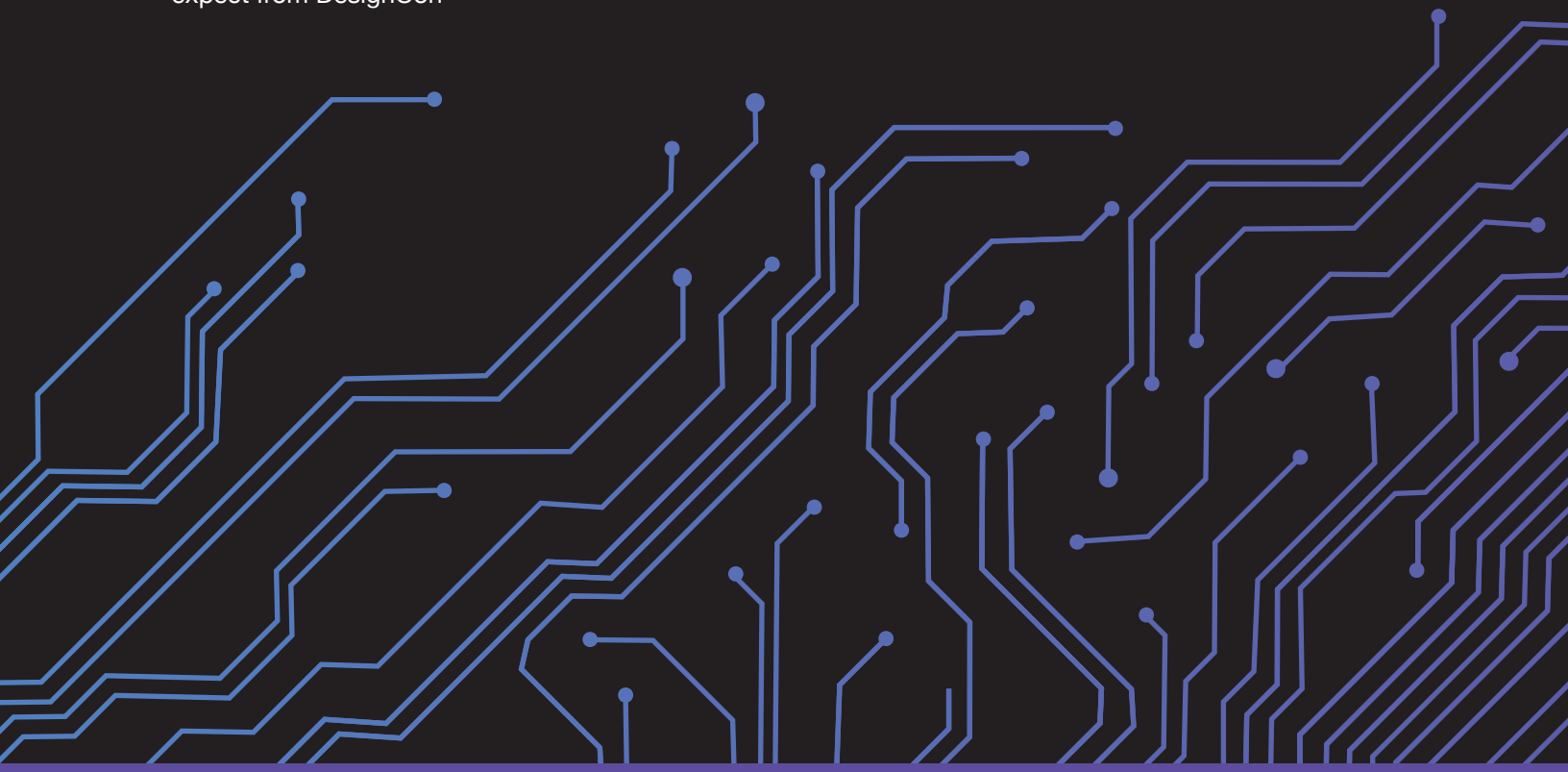

Find more information on **DesignCon.com** starting September 2021.

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