

## PRESS RELEASE

For Immediate Release

### **DesignCon Celebrates More than 40 Professionals with 2017 Awards for Best Papers**

*DesignCon 2018 Call for Papers Opens Mid-May*

**SAN FRANCISCO (April 18, 2017)** – DesignCon, the premier conference for chip, board and systems design engineers in the high-speed communications and semiconductor communities, announces the recipients of its Best Paper Awards following a successful DesignCon 2017 in Santa Clara, CA, on January 19-21. The winners are recognized for their outstanding contribution to the diverse educational goals of DesignCon. **To view the full list of winners, visit: <http://ubm.io/2pvrEHk>**

The 2017 DesignCon Best Paper Award winners have been selected through a two-step review process. First, the DesignCon Technical Program Committee, which is comprised of leading experts in the electronic design space, reviewed all papers for impact, relevance, quality, and originality. The first-round finalists were then judged based on attendee feedback, collected at DesignCon 2017, on the impact of their presentation.

“Congratulations to all finalists and winners of this year’s Best Paper Awards. UBM is pleased to recognize these outstanding papers as the best of the excellent content that DesignCon offers its attendees,” said Naomi Price, DesignCon Conference Content Director. “Each year, this awards program inspires engineers to strive to produce ground-breaking, top-tier content for the technical sessions at DesignCon.”

Winning papers cover four categories of design: Chip-Level Design, Board/System-Level Design, Serial Link Design, and Power & RF Design. A list of the winners is below:

#### **Chip-Level Design**

- *Characterizing and Selecting the VRM*  
Steve Sandler, Picotest

#### **Board/System-Level Design**

- *FastBER: A Novel Statistical Method for Arbitrary Transmitter Jitter*  
Yunhui Chu, Intel Corporation  
Alaeddin Aydiner, Intel Corporation  
Kai Xiao, Intel Corporation  
Beomtaek Lee, Intel Corporation  
Dan Oh, Samsung Electronics  
Oleg Mikulchenko, Intel Corporation  
Adam Norman, Intel Corporation  
Rob Friar, Intel Corporation  
Charles Phares, Intel Corporation
- *Non-Destructive Analysis and EM Model Tuning of PCB Signal Traces using the Beatty Standard*  
Heidi Barnes, Keysight Technologies  
José Moreira, Advantest  
Manuel Walz, Advantest
- *RX IBIS-AMI Model Silicon Correlation Metrics and Model Development Methodology*  
Masashi Shimanouchi, Intel Corporation  
Hsinho Wu, Intel Corporation  
Mike Peng Li, Intel Corporation

### **Serial Link Design**

- *Exploring Efficient Variability-Aware Analysis Method for High-Speed Digital Link Design Using PCE*  
Jan B. Preibisch, Technische Universität Hamburg-Harburg  
Torsten Reuschel, Technische Universität Hamburg-Harburg  
Katharina Scharff, Technische Universität Hamburg-Harburg  
Jayaprakash Balachandran, Cisco Systems Inc.  
Bidyut Sen, Cisco Systems Inc.  
Christian Schuster, Technische Universität Hamburg-Harburg
- *Investigation of Mueller-Muller CDR Algorithms in PAM4 High speed Serial Links*  
Yuhan Yao, Oracle Corporation  
Xun Zhang, Oracle Corporation  
Dawei Huang, Oracle Corporation  
Jianghui Su, Oracle Corporation  
Muthukumar Vairavan, Oracle Corporation  
Chai Palusa, Oracle Corporation
- *PCIe Gen4 Standards Margin Assisted Outer Layer Equalization for Cross Lane Optimization in a 16GT/s PCIe Link*  
Mohammad S. Mobin, Broadcom Ltd  
Haitao Xia, Broadcom Ltd  
Aravind Nayak, Broadcom Ltd  
Gene Saghi, Broadcom Ltd  
Christopher Abel, Broadcom Ltd  
Lane Smith, Broadcom Ltd  
Jun Yao, Broadcom Ltd

### **Power & RF Design**

- *Cost-effective PCB Material Characterization for High-volume Production Monitoring*  
Yongjin Choi, Hewlett-Packard Enterprise  
Christopher Cheng, Hewlett-Packard Enterprise  
Yasin Damgaci, Hewlett-Packard Enterprise  
Nagaraj Godishala, Hewlett-Packard Enterprise  
Yuriy Shlepnev, Simberian
- *Overview and Comparison of Power Converter Stability Metrics*  
Joseph 'Abe' Hartman, Oracle  
Alejandro 'Alex' Miranda, Oracle  
Kavitha Narayandass, Oracle  
Alexander Nosovitski, Oracle  
Istvan Novak, Oracle
- *RFI and Receiver Sensitivity Analysis in Mobile Electronic Devices*  
Antonio Ciccomancini Scogna, Samsung Electronics Mobile Division, HE Group  
Hwanwoo Shim, Samsung Electronics Mobile Division, HE Group  
Jiheon Yu, Samsung Electronics Mobile Division, HE Group  
Chang-Yong Oh, Samsung Electronics Mobile Division, HE Group  
Seyoon Cheon, Samsung Electronics Mobile Division, HE Group  
NamSeok Oh, Samsung Electronics Mobile Division, HE Group  
Dong Sub Kim, Samsung Electronics Mobile Division, HE Group

**To view the entire list of recipients, including individual researchers, please visit:**

**<http://designcon.com/santaclara/conference/paper-award-winners>**

### **DesignCon 2018 Call for Papers**

DesignCon returns to the Santa Clara Convention Center on January 30- February 1, 2018. Call for Papers will begin in mid-May with submissions due by the mid-July, 2017 deadline. To stay updated on next year's event, visit: [designcon.com](http://designcon.com)

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**Media Contacts:**

Jannelle Grigsby, [DesignConPR@ubm.com](mailto:DesignConPR@ubm.com), (310) 857-9020

Rich Trunzo, [DesignConPR@ubm.com](mailto:DesignConPR@ubm.com), (424) 316-7169

**About DesignCon**

DesignCon is the world's premier conference for chip, board and systems design engineers in the high-speed communications and semiconductor communities. DesignCon, created by engineers for engineers, takes place annually in Silicon Valley and remains the largest gathering of chip, board and systems designers in the country. This three-day technical conference and expo combines technical paper sessions, tutorials, industry panels, product demos and exhibits from the industry's leading experts and solutions providers. More information is available at: [designcon.com/santaclara](http://designcon.com/santaclara). DesignCon is organized by UBM Americas, a part of UBM plc (UBM.L), an Events First marketing and communications services business. For more information, visit [ubmamericas.com](http://ubmamericas.com).

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